

The MIPS32® 24Kc™ core from MIPS Technologies is a high-performance, low-power, 32-bit MIPS RISC core designed for custom system-on-silicon applications. The core is designed for semiconductor manufacturing companies, ASIC developers, and system OEMs who want to rapidly integrate their own custom logic and peripherals with a high-performance RISC processor. Fully synthesizable and highly portable across processes, it can be easily integrated into full system-on-silicon designs, allowing developers to focus their attention on end-user products.

The 24Kc core implements the MIPS32 Release 2 Architecture in an 8-stage pipeline. It includes support for the MIPS16e™ application specific extension and the 32-bit privileged resource architecture. This standard architecture allows support by a wide range of industry standard tools and development systems.

To maintain high pipeline utilization, dynamic branch prediction is included in the form of a Branch History Table and a Return Prediction Stack. The Memory Management Unit (MMU) contains 4-entry instruction and 8-entry data Translation Lookaside Buffers (ITLB/DTLB) and a configurable 16/32/64 dual-entry joint TLB (JTLB) with variable page sizes. Alternatively, for applications not requiring address mapping or protection, the TLBs can be replaced with a simple Fixed Mapping mechanism.

The synthesizable 24Kc core includes a high performance Multiply/Divide Unit (MDU). The MDU is fully pipelined to support a single cycle repeat rate for 32x32 MAC instructions, which enables multiply-intensive algorithms to be performed efficiently. Further, in the 24Kc Pro™ Core, the optional CorExtend block can utilize the HI/LO registers in the MDU block. The CorExtend block allows specialized functions to be efficiently implemented.

Instruction and data level-one caches are configurable at 0, 16, 32, or 64 KB in size. Each cache is organized as 4-way set associative. Data cache misses are non-blocking and up to 4 may be outstanding. Two instruction cache misses can be outstanding. Both caches are virtually indexed and physically tagged to allow them to be accessed in the same cycle that the address is translated. To achieve high frequencies while using commercially available SRAM generators, the cache access is spread across two pipeline stages, leaving nearly an entire cycle for the SRAM access.

The Bus Interface Unit implements the Open Core Protocol (OCP) which has been developed to address the needs of SOC designers. This implementation features 64-bit read and write data buses to efficiently transfer data to and from the L1 caches. The BIU also supports a variety of core/bus clock ratios to give greater flexibility for system design implementations.

Optional interfaces are supported to external scratchpad or coprocessor blocks.

An Enhanced JTAG (EJTAG) version 3.10 compliant block allows for software debugging of the processor and includes a TAP controller as well as optional instruction and data virtual address/value breakpoints. Additionally, real-time tracing of instruction program counter, data address and data values can be supported.

Figure 1 shows a block diagram of the 24Kc core.

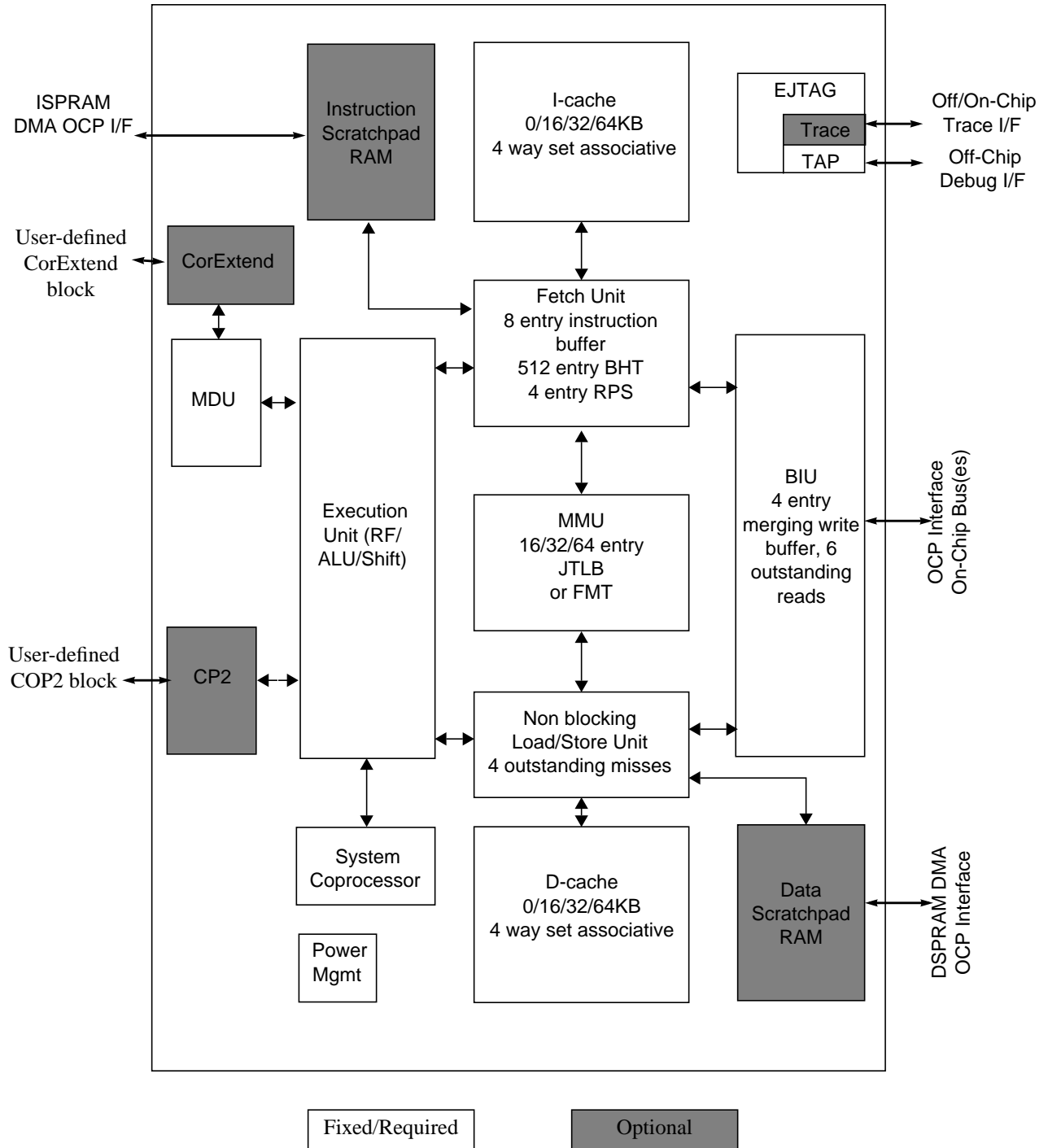


Figure 1 24Kc™ Core Block Diagram

## 24Kc™ Core Features

- 8-stage pipeline
- 32-bit address paths
- 64-bit data paths to caches and external interface
- MIPS32-Compatible Instruction Set
  - Multiply-Accumulate and Multiply-Subtract Instructions (MADD, MADDU, MSUB, MSUBU)
  - Targeted Multiply Instruction (MUL)
  - Zero/One Detect Instructions (CLZ, CLO)
  - Wait Instruction (WAIT)
  - Conditional Move Instructions (MOVZ, MOVN)
  - Prefetch Instruction (PREF)
- MIPS32 Enhanced Architecture (Release 2) Features
  - Vectored interrupts and support for external interrupt controller
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)
  - Bit field manipulation instructions
- MIPS32 Privileged Resource Architecture
- Programmable Memory Management Unit
  - 16/32/64 dual-entry JTLB with variable page sizes
  - 4-entry ITLB
  - 8-entry DTLB
  - Optional simple Fixed Mapping Translation (FMT) mechanism
- MIPS16e™ Code Compression
  - 16 bit encodings of 32 bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8 and 16 bit datatypes
- Programmable L1 Cache Sizes
  - Individually configurable instruction and data caches
  - Instruction and Data cache sizes of 0/16/32/64 KB
  - 4-Way Set Associative
  - Up to 4 outstanding load misses
  - Write-back and write-through support
  - 32-byte cache line size
  - Virtually indexed, physically tagged
  - Cache line locking support
  - Non-blocking prefetches
  - Optional parity support
- Bus Interface
  - OCP 2.1 compliant
  - OCP interface with 32-bit address and 64-bit data
  - OCP interface runs at core/bus clock ratios of 1, 1.5, 2, 2.5, 3, 3.5, 4 or 5 via a separate synchronous bus clock
  - Burst size of four 64-bit beats
  - 4 entry write buffer
  - “Simple” byte enable mode allows easier bridging to other bus standards
  - Extensions for front-side L2 cache
- Scratchpad RAM support
  - Independent Instruction and Data Scratchpad RAM
  - Independent of cache configuration
  - Independent 64 bit OCP interface for external DMA
  - External interface runs at the same core/bus clock ratio as that of BIU interface
  - Maximum size of 1MB each
  - Interface allows back-stalling the core
- Multiply/Divide Unit
  - Maximum issue rate of one 32x32 multiply per clock
  - 5 cycle multiply latency
  - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (*rs*) sign extension-dependent)
- CorExtend™ User Defined Instruction Set Extensions (available in 24Kc Pro™ core)
  - Allows user to define and add instructions to the core at build time
  - Maintains full MIPS32 compatibility
  - Supported by industry standard development tools
  - Single or multi-cycle instructions
  - Separately licensed; a core with this feature is known as the 24Kc Pro™ core
  - Implemented in same block as MDU, allows HI and LO registers to be shared for MIPS32 and CorExtend multiply operations.
- Coprocessor 2 interface
  - 64 bit interface to a user designed coprocessor
- Power Control
  - Minimum frequency: 0 MHz
  - Power-down mode (triggered by WAIT instruction)
  - Support for software-controlled clock divider
  - Support for extensive use of local gated clocks
- EJTAG Debug
  - Support for single stepping
  - Virtual instruction and data address/value breakpoints
  - TAP controller is chainable for multi-CPU debug
  - Cross-CPU breakpoint support
  - EJTAG version 3.10 compliant
- MIPS Trace
  - PC, data address and data value tracing w/ trace compression
  - Support for on-chip and off-chip trace memory

- PDTrace version 4.1 compliant
- Testability
  - Full scan design achieves test coverage in excess of 99% (dependent on library and configuration options)
  - Optional memory BIST for internal SRAM arrays

## Architecture Overview

The 24Kc core contains a variety of blocks some of which are always present, while others are optional.

The required blocks are as follows:

- Fetch Unit
- Execution Unit
- MIPS16e recode
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Cache Controllers
- Bus Interface Unit (BIU)
- Power Management
- Instruction Cache

Optional blocks include:

- CorExtend™ User Defined Instruction (UDI) support
- Enhanced JTAG (EJTAG) breakpoints
- MIPS Trace (PDTrace) support
- Instruction/Data cache
- Instruction/Data scratchpad
- COP2 interface

## Pipeline Flow

The 24Kc core implements an 8-stage pipeline. Three extra fetch stages are conditionally added when executing MIPS16e instructions. This pipeline allows the processor to achieve a high frequency while maintaining reasonable area and power numbers.

The 24Kc core pipeline consists of the following stages:

- IF - Instruction Fetch First
- IS - Instruction Fetch Second
- IR - Instruction Recode (MIPS16e only)
- IK - Instruction Kill (MIPS16e only)

- IT - Instruction Fetch Third (MIPS16e only)
- RF - Register File access
- AG - Address Generation
- EX - Execute
- MS - Memory Second
- ER - Exception Resolution
- WB - WriteBack

The 24Kc core implements a bypass mechanism that allows the result of an operation to be forwarded directly to the instruction that needs it without having to write the result to the register and then read it back.

Figure 2 shows a diagram of the 24Kc core pipeline.

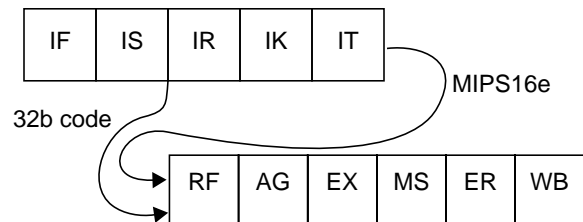


Figure 2 24Kc™ Core Pipeline

### IF Stage: Instruction Fetch First

- I-cache tag/data arrays accessed
- Branch History Table accessed
- ITLB address translation performed
- Instruction watch and EJTAG break compares done

### IS - Instruction Fetch Second

- Detect I-cache hit
- Way select
- MIPS32 Branch prediction

### IR - Instruction Recode

- MIPS16e instruction recode
- MIPS16e branch prediction

### IK - Instruction Kill

- MIPS16e instruction kill

### IT - Instruction Fetch Third

- Instruction Buffer

- Branch target calculation

#### **RF - Register File Access**

- Register File access
- Instruction decoding/dispatch logic
- Bypass muxes

#### **AG - Address Generation**

- D-cache Address Generation
- Bypass muxes

#### **EX - Execute/Memory Access**

- Skewed ALU
- DTLB
- Start DCache access
- Branch Resolution
- Data watch and EJTAG break address compares

#### **MS - Memory Access Second**

- Complete DCache access
- DCache hit detection
- Way select mux
- Load align
- EJTAG break data value compare

#### **ER- Exception Resolution**

- Instruction completion
- Register file write setup
- Exception processing

#### **WB - Writeback**

- Register file writeback occurs on rising edge of this cycle

### **24Kc™ Core Logic Blocks**

The 24Kc core consists of the following logic blocks, shown in [Figure 1](#). These logic blocks are defined in the following subsections:

- Fetch Unit
- Execution Unit
- MIPS16e support
- System Control Coprocessor (CP0)

- Memory Management Unit (MMU)
- Cache Controller
- Bus Interface Unit (BIU)
- Power Management

#### **Fetch Unit**

The 24Kc core fetch unit is responsible for fetching instructions and providing them to the rest of the pipeline, as well as handling control transfer instructions (branches, jumps, etc.). It calculates the address for each instruction fetch and contains an instruction buffer that decouples the fetching of instructions from their execution.

The fetch unit contains two structures for the dynamic prediction of control transfer instructions. A 512-entry Branch History Table (BHT) is used to predict the direction of branch instructions. It uses a bimodal algorithm with two bits of history information per entry. Also, a 4-entry Return Prediction Stack (RPS) is a simple structure to hold the return address from the most recent subroutine calls. The link address is pushed onto the stack whenever a JAL, JALR, or BGEZAL instruction is seen. Then that address is popped when a JR instruction occurs.

#### **Execution Unit**

The 24Kc core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The 24Kc core contains thirty-two 32-bit general-purpose registers used for integer operations and address calculation. Optionally, one or three additional register file shadow sets (each containing thirty-two registers) can be added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Logic for verifying branch prediction
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instructions streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions

- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter & Store Aligner

### MIPS16e™ Application Specific Extension

The 24Kc core includes support for the MIPS16e ASE. This ASE improves code density through the use of 16-bit encoding of many MIPS32 instructions plus some MIPS16e-specific instructions. PC relative loads allow quick access to constants. Save/Restore macro instructions provide for single instruction stack frame setup/teardown for efficient subroutine entry/exit.

### Multiply/Divide Unit (MDU)

The 24Kc core includes a multiply/divide unit (MDU) that contains a separate pipeline for integer multiply and divide operations. This pipeline operates in parallel with the integer unit pipeline and does not stall when the integer pipeline stalls. This allows any long-running MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The MDU consists of a pipelined 32x32 multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic.

The MDU supports execution of one multiply or multiply accumulate operation every clock cycle.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit-wide *rs*, 15 iterations are skipped, and for a 24-bit-wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes a pipeline stall until the divide operation is completed.

Table 1 lists the latencies (number of cycles until a result is available) and repeat rates (peak issue rate of cycles until the operation can be reissued) for the 24Kc core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks. For a more detailed discussion of latencies and repeat rates, refer to Chapter 2 of the *MIPS32 24K Processor Core Family Software User's Manual*.

Table 1 24Kc™ Core Integer Multiply/Divide Unit Latencies and Repeat Rates

Opcode	Operand Size (mul <i>rt</i> ) (div <i>rs</i> )	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU, MSUB/MSUBU	32 bits	5	1
MUL	32 bits	5	1 <sup>1</sup>
DIV/DIVU	8 bits	12/14	12/14
	16 bits	20/22	20/22
	24 bits	28/30	28/30
	32 bits	36/38	36/38

1.If there is no data dependency, a MUL can be issued every cycle.

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the general-purpose register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair.

Two other instructions, multiply-add (MADD) and multiply-subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

### System Control Coprocessor (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation and cache protocols, the exception control system, the processor's diagnostic capability, the operating modes (kernel, user, supervisor, and debug), and whether interrupts are enabled or disabled. Configuration information, such as cache size and associativity, presence of features like MIPS16e or floating point unit, is also available by accessing the CP0 registers, listed in Table 2.

Table 2 Coprocessor 0 Registers in Numerical Order

Register Number	Register Name	Function
0	Index <sup>3</sup>	Index into the TLB array.
1	Random <sup>3</sup>	Randomly generated index into the TLB array.
2	EntryLo0 <sup>3</sup>	Low-order portion of the TLB entry for even-numbered virtual pages.
3	EntryLo1 <sup>3</sup>	Low-order portion of the TLB entry for odd-numbered virtual pages.
4	Context <sup>1</sup>	Pointer to page table entry in memory.
5	PageMask <sup>3</sup>	Control for variable page sizes in TLB entries.
6	Wired <sup>3</sup>	Controls the number of fixed (“wired”) TLB entries.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr <sup>1</sup>	Reports the address for the most recent address-related exception.
9	Count <sup>1</sup>	Processor cycle count.
10	EntryHi <sup>3</sup>	High-order portion of the TLB entry.
11	Compare <sup>1</sup>	Timer interrupt control.
12	Status <sup>1</sup>	Processor status and control.
12	IntCtl <sup>1</sup>	Interrupt system status and control.
12	SRSCtl <sup>1</sup>	Shadow register set status and control.
12	SRSMap <sup>1</sup>	Provides mapping from vectored interrupt to a shadow set.
13	Cause <sup>1</sup>	Cause of last general exception.
14	EPC <sup>1</sup>	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration register 1.

Table 2 Coprocessor 0 Registers in Numerical Order

Register Number	Register Name	Function
16	Config2	Configuration register 2.
16	Config3	Configuration register 3.
16	Config7	Configuration register 7.
17	Reserved	Reserved in the 24Kc core.
18	WatchLo <sup>1</sup>	Low-order watchpoint address.
19	WatchHi <sup>1</sup>	High-order watchpoint address.
20-22	Reserved	Reserved in the 24Kc core.
23	Debug <sup>2</sup>	Debug control and exception status.
23	Trace Control <sup>2</sup>	PC/Data trace control register.
23	Trace Control2 <sup>2</sup>	Additional PC/Data trace control.
23	User Trace Data <sup>2</sup>	User Trace control register.
23	TraceBPC <sup>2</sup>	Trace breakpoint control.
24	DEPC <sup>2</sup>	Program counter at last debug exception.
25	PerfCount	Performance counters and associated control.
26	ErrCtl	Used for software testing of cache arrays.
27	CacheErr	Cache parity error interface.
28	TagLo/ DataLo	Low-order portion of cache tag interface.
29	DataHi	Hi-order portion of cache tag interface.
30	ErrorEPC <sup>1</sup>	Program counter at last error.
31	DESAVE <sup>2</sup>	Debug handler scratchpad register.
1. Registers used in exception processing. 2. Registers used during debug. 3. Registers used in memory management.		

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events, or program errors. Table 3 shows the exception types in order of priority.

Table 3 24Kc™ Core Exception Types

Exception	Description
Reset	Assertion of <i>SI_Reset</i> signal.
DSS	EJTAG Debug Single Step.
DINT	EJTAG Debug Interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input, or by setting the <i>EjtagBrk</i> bit in the ECR register.
DDBLImpr/ DDBSImpr	Debug Data Break Load/Store Imprecise
NMI	Assertion of <i>SI_NMI</i> signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
Deferred Watch	Deferred Watch (unmasked by $K DM \rightarrow !(K DM)$ transition).
DIB	EJTAG debug hardware instruction break matched.
WATCH	A reference to an address in one of the watch registers (fetch).
AdEL	Fetch address alignment error. Fetch reference to protected address.
TLBL	Fetch TLB miss.
TLBL	Fetch TLB hit to page with V=0.
I Cache Error	Instruction cache parity error
IBE	Instruction fetch bus error.
DBp	EJTAG Breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Bp	Execution of BREAK instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
RI	Execution of a Reserved Instruction.
C2E	Coprocessor2 Exception
IS1	Implementation specific Coprocessor2 exception
Ov	Execution of an arithmetic instruction that overflowed.

Table 3 24Kc™ Core Exception Types (Continued)

Exception	Description
Tr	Execution of a trap (when trap condition is true).
Machine Check	TLB write that conflicts with an existing entry.
DDBL / DDBS	EJTAG Data Address Break (address only).
WATCH	A reference to an address in one of the watch registers (data).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
TLBL	Load TLB miss.
TLBL	Load TLB hit to page with V=0.
TLBS	Store TLB miss.
TLBS	Store TLB hit to page with V=0.
TLB Mod	Store to TLB page with D=0.
D Cache Error	Data cache parity error - imprecise
DBE	Load or store bus error - imprecise

### Interrupt Handling

The 24Kc core includes support for six hardware interrupt pins, two software interrupts, a timer interrupt, and a performance counter interrupt. These interrupts can be used in any of three interrupt modes, as defined by Release 2 of the MIPS32 Architecture:

- Interrupt compatibility mode, which acts identically to that in an implementation of Release 1 of the Architecture.
- Vectored Interrupt (VI) mode, which adds the ability to prioritize and vector interrupts to a handler dedicated to that interrupt, and to assign a GPR shadow set for use during interrupt processing. The presence of this mode is denoted by the *VInt* bit in the *Config3* register. This mode is architecturally optional; but it is always present on the 24Kc core, so the *VInt* bit will always read as a 1 for the 24Kc core.
- External Interrupt Controller (EIC) mode, which redefines the way in which interrupts are handled to provide full support for an external interrupt controller handling prioritization and vectoring of interrupts. This



presence of this mode denoted by the VEIC bit in the *Config3* register. Again, this mode is architecturally optional. On the 24Kc core, the VEIC bit is set externally by the static input, *SI\_EICPresent*, to allow system logic to indicate the presence of an external interrupt controller.

The reset state of the processor is to interrupt compatibility mode such that a processor supporting Release 2 of the Architecture, like the 24Kc core, is fully compatible with implementations of Release 1 of the Architecture.

VI or EIC interrupt modes can be combined with the optional shadow registers to specify which shadow set should be used upon entry to a particular vector. The shadow registers further improve interrupt latency by avoiding the need to save context when invoking an interrupt handler.

### GPR Shadow Registers

Release 2 of the MIPS32 Architecture optionally removes the need to save and restore GPRs on entry to high priority interrupts or exceptions, and to provide specified processor modes with the same capability. This is done by introducing multiple copies of the GPRs, called *shadow sets*, and allowing privileged software to associate a shadow set with entry to kernel mode via an interrupt vector or exception. The normal GPRs are logically considered shadow set zero.

The number of GPR shadow sets is a build-time option on the 24Kc core. Although Release 2 of the Architecture defines a maximum of 16 shadow sets, the core allows one (the normal GPRs), two, or four shadow sets. The highest number actually implemented is indicated by the *SRSCtl<sub>HSS</sub>* field. If this field is zero, only the normal GPRs are implemented.

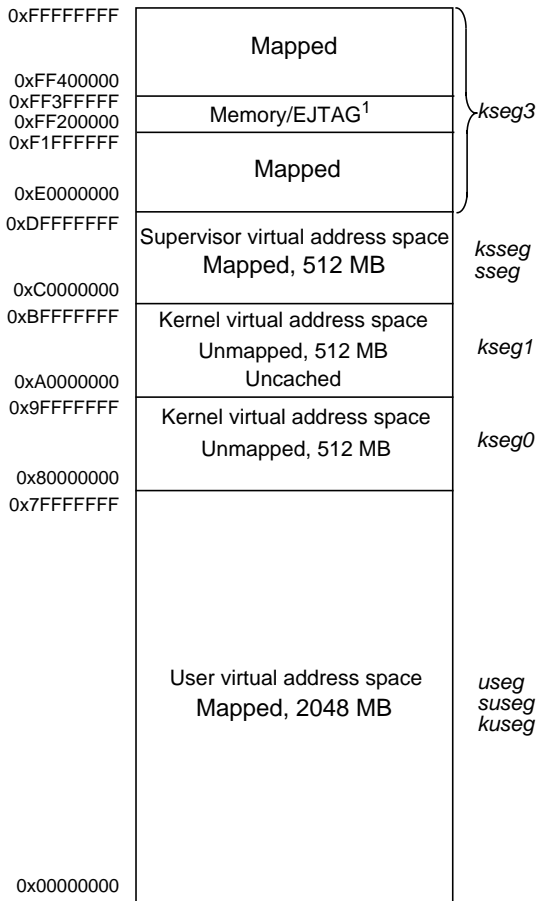
Shadow sets are new copies of the GPRs that can be substituted for the normal GPRs on entry to kernel mode via an interrupt or exception. Once a shadow set is bound

to a kernel mode entry condition, reference to GPRs work exactly as one would expect, but they are redirected to registers that are dedicated to that condition. Privileged software may need to reference all GPRs in the register file, even specific shadow registers that are not visible in the current mode. The *RDPGPR* and *WRPGPR* instructions are used for this purpose. The *CSS* field of the *SRSCtl* register provides the number of the current shadow register set, and the *PSS* field of the *SRSCtl* register provides the number of the previous shadow register set (that which was current before the last exception or interrupt occurred).

If the processor is operating in VI interrupt mode, binding of a vectored interrupt to a shadow set is done by writing to the *SRSMap* register. If the processor is operating in EIC interrupt mode, the binding of the interrupt to a specific shadow set is provided by the external interrupt controller, and is configured in an implementation-dependent way. Binding of an exception or non-vectored interrupt to a shadow set is done by writing to the *ESS* field of the *SRSCtl* register. When an exception or interrupt occurs, the value of *SRSCtl<sub>CSS</sub>* is copied to *SRSCtl<sub>PSS</sub>*, and *SRSCtl<sub>CSS</sub>* is set to the value taken from the appropriate source. On an *ERET*, the value of *SRSCtl<sub>PSS</sub>* is copied back into *SRSCtl<sub>CSS</sub>* to restore the shadow set of the mode to which control returns.

### Modes of Operation

The 24Kc core supports four modes of operation: user mode, supervisor mode, kernel mode, and debug mode. User mode is most often used for application programs. Supervisor mode gives an intermediate privilege level with access to the *ksseg* address space. Supervisor mode is not supported with the fixed mapping MMU. Kernel mode is typically used for handling exceptions and operating system kernel functions, including *CP0* management and I/O device accesses. An additional Debug mode is used during system bring-up and software development. Refer to "[EJTAG Debug Support](#)" on page 23 for more information on debug mode.



1. This space is mapped to memory in kernel mode, and by the EJTAG module in debug mode.

Figure 3 24Kc™ Core Virtual Address Map

## Memory Management Unit (MMU)

The 24Kc core contains a configurable Memory Management Unit (MMU) that is primarily responsible for converting virtual addresses to physical addresses and providing attribute information for different segments of memory.

Two types of MMUs are possible on the 24Kc core, selectable when the core is synthesized. Software can identify the type of MMU present by querying the MT field of the *Config* register.

1. Translation Lookaside Buffer (TLB) -style MMU. The basic TLB functionality is specified by the MIPS32 Privileged Resource Architecture (PRA). A TLB provides mapping and protection capability with

per-page granularity. The 24Kc implementation allows a wide range of page sizes to be present simultaneously.

2. Fixed Mapping Translation (FMT) -style MMU. The FMT is much simpler and smaller than the TLB-style MMU, and is a good choice when the full protection and flexibility of the TLB is not needed.

## Translation Lookaside Buffer (TLB)

The TLB consists of three address translation buffers:

- 16/32/64 dual-entry fully associative Joint TLB (JTLB)
- 4-entry fully associative Instruction Micro TLB (ITLB)
- 8-entry fully associative Data Micro TLB (DTLB)

When an instruction or data address is calculated, the virtual address is compared to the contents of the appropriate micro TLB (uTLB). If the address is not found in the ITLB or DTLB, the JTLB is accessed. If the entry is found in the JTLB, that entry is then written into the uTLB. If the address is not found in the JTLB, a TLB exception is taken.

Figure 4 shows how the ITLB, DTLB, and JTLB are implemented in the 24Kc core.

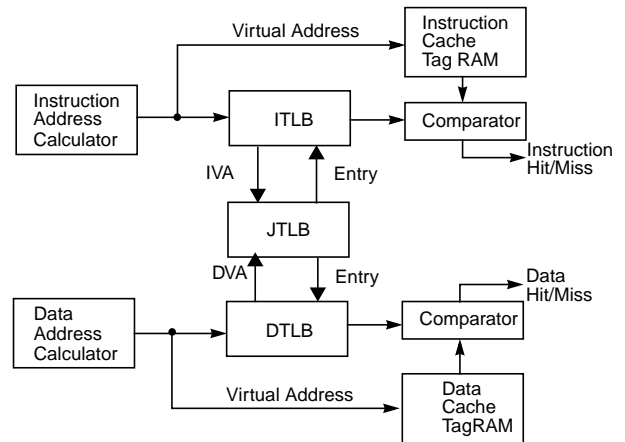


Figure 4 Address Translation During a Cache Access

## Joint TLB (JTLB)

The 24Kc core implements a fully associative JTLB containing 16, 32, or 64-dual-entries mapping up to 128 virtual pages to their corresponding physical addresses. The purpose of the TLB is to translate virtual addresses and their corresponding ASIDs into a physical memory address. The translation is performed by comparing the upper bits of the virtual address (along with the ASID)

against each of the entries in the *tag* portion of the joint TLB structure.

The JTLB is organized as pairs of even and odd entries containing pages that range in size from 4 KB to 256 MB, in factors of four, into the 4 GB physical address space. The JTLB is organized in page pairs to minimize the overall size. Each *tag* entry corresponds to two data entries: an even page entry and an odd page entry. The highest order virtual address bit not participating in the tag comparison is used to determine which of the data entries is used. Since page size can vary on a page-pair basis, the determination of which address bits participate in the comparison and which bit is used to make the even-odd determination is decided dynamically during the TLB look-up.

### Instruction TLB (ITLB)

The ITLB is a small 4-entry, fully associative TLB dedicated to performing translations for the instruction stream. The ITLB only maps 4 KB or 1 MB pages/subpages. For 4 KB or 1 MB pages, the entire page is mapped in the ITLB. If the main TLB page size is between 4 KB and 1 MB, only the current 4 KB subpage is mapped.

Similarly, for page sizes larger than 1 MB, the current 1 MB subpage is mapped.

The ITLB is managed by hardware and is transparent to software. The larger JTLB is used as a backing structure for the ITLB. If a fetch address cannot be translated by the ITLB, the JTLB is used to attempt to translate it in the following clock cycle, or when available. If successful, the translation information is copied into the ITLB for future use. There is a minimum two cycle ITLB miss penalty.

### Data TLB (DTLB)

The DTLB is a small 8-entry, fully associative TLB dedicated to performing translations for loads and stores. Similar to the ITLB, the DTLB only maps either 4 KB or 1 MB pages/subpages.

The DTLB is managed by hardware and is transparent to software. The larger JTLB is used as a backing structure for the DTLB. If a load/store address cannot be translated by the DTLB, a lookup is done in the JTLB. If the JTLB translation is successful, the translation information is copied into the DTLB for future use. The DTLB miss penalty is also two cycles.

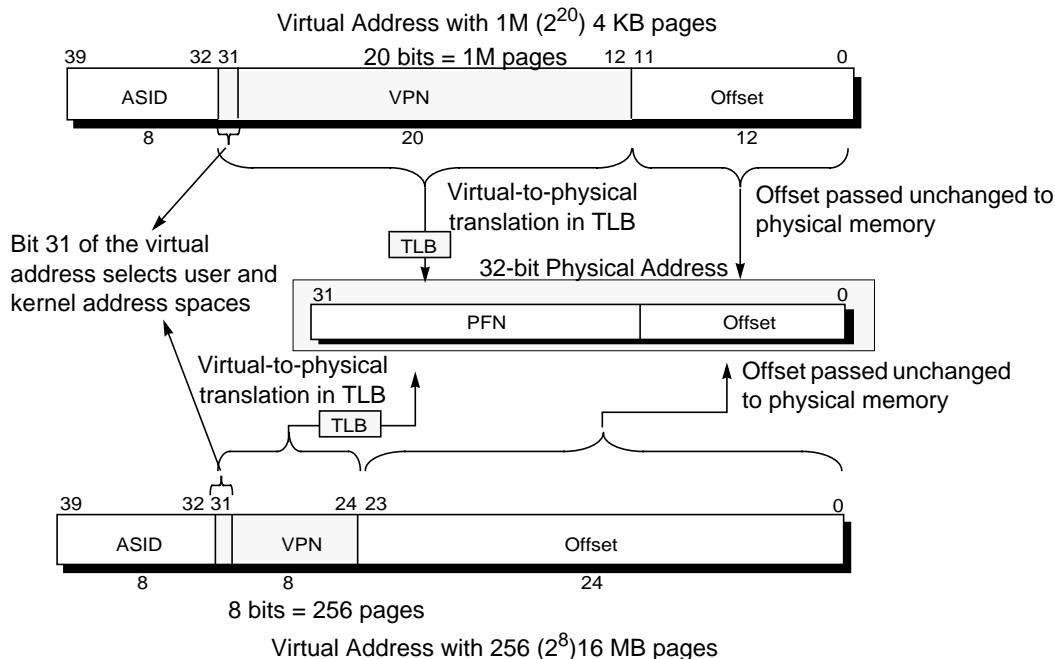


Figure 5 32-bit Virtual Address Translation

## Virtual-to-Physical Address Translation

Converting a virtual address to a physical address begins by comparing the virtual address from the processor with the virtual addresses in the TLB; there is a match when the virtual page number (VPN) of the address is the same as the VPN field of the entry, and either:

- The Global (*G*) bit of the TLB entry is set, or
- The ASID field of the virtual address is the same as the ASID field of the TLB entry.

This match is referred to as a TLB *hit*. If there is no match, a TLB *miss* exception is taken by the processor and software is allowed to refill the TLB from a page table of virtual/physical addresses in memory.

Figure 5 shows a flow diagram of the address translation process for two different page sizes.

The top portion of Figure 5 shows a virtual address for a 4 KB page size. The width of the *Offset* in Figure 5 is defined by the page size. The remaining 20 bits of the address represent the virtual page number (*VPN*), and index the 1M-entry page table.

The bottom portion of Figure 5 shows the virtual address for a 16 MB page size. The remaining 8 bits of the address represent the VPN, and index the 256-entry page table.

In Figure 5, the virtual address is extended with an 8-bit address space identifier (ASID), which reduces the frequency of TLB flushes during context switches. This 8-bit ASID contains the number assigned to that process and is stored in the CP0 *EntryHi* register.

### Hits, Misses, and Multiple Matches

Each JTLB entry contains a tag portion and a data portion. If a match is found, the upper bits of the virtual address are replaced with the page frame number (PFN) stored in the corresponding entry in the data array of the joint TLB (JTLB). The granularity of JTLB mappings is defined in terms of TLB *pages*. The 24Kc core's JTLB supports pages of different sizes ranging from 4 KB to 256 MB in factors of 4.

Table 4 shows the address bits used for even/odd bank selection depending on page size and the relationship between the legal values in the mask register and the selected page size.

Table 4 Mask and Page Size Values

Pagemask[28:13]	Page Size	Even/Odd Bank Select Bit
0000000000000000	4KB	VAddr[12]
0000000000000011	16KB	VAddr[14]
0000000000001111	64KB	VAddr[16]
0000000001111111	256KB	VAddr[18]
0000000111111111	1MB	VAddr[20]
0000011111111111	4MB	VAddr[22]
0001111111111111	16MB	VAddr[24]
0011111111111111	64MB	VAddr[26]
1111111111111111	256MB	VAddr[28]

If no match occurs (TLB miss), an exception is taken and software refills the TLB from the page table resident in memory. Software can write over a selected TLB entry or use a hardware mechanism to write into a random entry.

The 24Kc core implements a TLB write compare mechanism to ensure that multiple TLB matches do not occur. On the TLB write operation, the write value is compared with all other entries in the TLB. If a match occurs, the 24Kc core takes a machine check exception, sets the TS bit in the CP0 *Status* register, and aborts the write operation.

Compared with previous cores from MIPS Technologies, the 24Kc core uses a more relaxed check for multiple matches in order to avoid machine check exceptions while flushing or initializing the TLB. On a write, all matching entries are disabled to prevent them from matching on future compares. A machine check is only signaled if the entry being written has its valid bit set, the matching entry in the TLB has its valid bit set, and the matching entry is not the entry being written.

### TLB Tag and Data Formats

Figure 6 shows the format of a TLB *tag* entry. The entry is divided into the follow fields:

- Global process indicator
- Address space identifier
- Virtual page number
- Compressed page mask

Setting the global process indicator (G bit) indicates that the entry is global to all processes and/or threads in the system. In this case, the 8-bit address space identifier (ASID) value is ignored since the entry is not relative to a specific thread or process.

The ASID field can help to reduce the frequency of TLB flushes on a context switches. The existence of the ASID allows multiple processes to exist in both the TLB and instruction caches. The current ASID value is stored in the *EntryHi* register and is compared to the ASID value of each entry. Figure 6 and Table 5 show the TLB tag entry format.

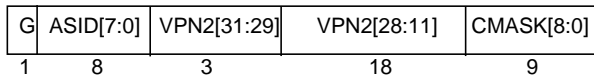


Figure 6 TLB Tag Entry Format

Table 5 TLB Tag Entry Fields

Field Name	Description
G	Global Bit. When set, indicates that this entry is global to all processes and/or threads and thus disables inclusion of the ASID in the comparison.
ASID[7:0]	Address Space Identifier. Identifies with which process or thread this TLB entry is associated.
VPN2[31:29], VPN2[28:13]	Virtual Page Number divided by 2. This field contains the upper bits of the virtual page number. Because it represents a pair of TLB pages, it is divided by 2. Bits 31:29 are always included in the TLB lookup comparison. Bits 28:13 are included depending on the page size.
CMASK[8:0]	Compressed page mask value. This field is a compressed version of the page mask. It defines the page size by masking the appropriate VPN2 bits from being involved comparison. It is also used to determine which address bit is used to make the even-odd page determination.

Figure 7 and Table 6 show the TLB data array entry format.

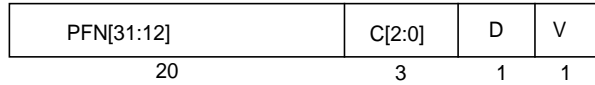


Figure 7 TLB Data Array Entry Format

Table 6 TLB Data Array Entry Fields

Field Name	Description														
PFN[31:12]	Physical Frame Number. Defines the upper bits of the physical address. For page sizes larger than the 4KB, only a subset of these bits is actually used.														
C[2:0]	Cacheability. Contains an encoded value of the cacheability attributes and determines whether the page should be placed in the cache or not. The field is encoded as follows: <table border="1" data-bbox="1003 772 1393 1136"> <thead> <tr> <th>CS[2:0]</th> <th>Coherency Attribute</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Cacheable, noncoherent, write through, no write allocate.</td> </tr> <tr> <td>1</td> <td>Reserved</td> </tr> <tr> <td>2</td> <td>Uncached</td> </tr> <tr> <td>3</td> <td>Cacheable, noncoherent, write back, write allocate</td> </tr> <tr> <td>4-6</td> <td>Reserved</td> </tr> <tr> <td>7</td> <td>Uncached Accelerated</td> </tr> </tbody> </table>	CS[2:0]	Coherency Attribute	0	Cacheable, noncoherent, write through, no write allocate.	1	Reserved	2	Uncached	3	Cacheable, noncoherent, write back, write allocate	4-6	Reserved	7	Uncached Accelerated
CS[2:0]	Coherency Attribute														
0	Cacheable, noncoherent, write through, no write allocate.														
1	Reserved														
2	Uncached														
3	Cacheable, noncoherent, write back, write allocate														
4-6	Reserved														
7	Uncached Accelerated														
D	“Dirty” or write-enable bit. Indicates that the page has been written and/or is writable. If this bit is set, stores to the page are permitted. If the bit is cleared, stores to the page cause a TLB Modified exception.														
V	Valid bit. Indicates that the TLB entry, and thus the virtual page mapping, are valid. If this bit is set, accesses to the page are permitted. If the bit is cleared, accesses to the page cause a TLB Invalid exception.														

## Page Sizes and Replacement Algorithm

To assist in controlling both the amount of mapped space and the replacement characteristics of various memory regions, the 24Kc core provides two mechanisms. First, the page size can be configured, on a per-entry basis, to map a page size from 4 KB to 256 MB (in multiples of 4). The CP0 *PageMask* register is loaded with the mapping page size, which is then entered into the TLB when a new entry is written. Thus, operating systems can provide special purpose maps. For example, a typical frame buffer might be memory mapped with only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. To select a TLB entry to be written with a new mapping, the 24Kc core provides a random replacement algorithm. However, the processor also provides a mechanism where a programmable number of mappings can be locked into the TLB via the CP0 *Wired* register, thus avoiding random replacement.

## Fixed Mapping Translation (FMT)

The 24Kc core optionally provides a Fixed Mapping Translation mechanism that is smaller and simpler than the full Translation Lookaside Buffer (TLB). Like a TLB, the FMT performs virtual-to-physical address translation and provides attributes for the different segments. Those segments that are unmapped in a TLB implementation (kseg0 and kseg1) are handled identically by the FMT.

Figure 8 shows how the FMT is implemented in the 24Kc core.

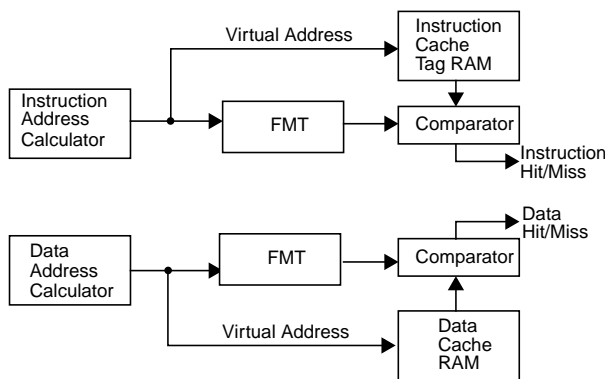


Figure 8 Address Translation During Access

In general, the FMT also determines the cacheability of each segment. These attributes are controlled via bits in the *Config* register. Table 7 shows the encoding for the K23 (bits 30:28), KU (bits 27:25), and K0 (bits 2:0) fields of the

Config register. Table 8 shows how the cacheability of the virtual address segments is controlled by these fields.

Table 7 Cache Coherency Attributes

Config Register Fields K23, KU, and K0	Cache Coherency Attribute
0	Cacheable, noncoherent, write-through, no write-allocate
1	Reserved
2	Uncached
3	Cacheable, noncoherent, write-back, write-allocate
4-6	Reserved
7	Uncached Accelerated

In a 24Kc core with FMT, no translation exceptions can be taken, although address errors are still possible.

Table 8 Virtual Address Segments

Segment	Virtual Address Range	Cacheability
useg kuseg	0x0000_0000- 0x7FFF_FFFF	Controlled by the KU field (bits 27:25) of the Config register. See Table 7 for mapping. This segment is always uncached when ERL = 1.
kseg0	0x8000_0000- 0x9FFF_FFFF	Controlled by the K0 field (bits 2:0) of the Config register. See Table 7 for mapping.
kseg1	0xA000_0000- 0xBFFF_FFFF	Always uncacheable.
kseg2	0xC000_0000- 0xDFFF_FFFF	Controlled by the K23 field (bits 30:28) of the Config register. See Table 7 for mapping.
kseg3	0xE000_0000- 0xFFFF_FFFF	Controlled by the K23 field (bits 30:28) of the Config register. See Table 7 for mapping.

The FMT performs a simple translation to map from virtual addresses to physical addresses. This mapping is shown in Figure 9.

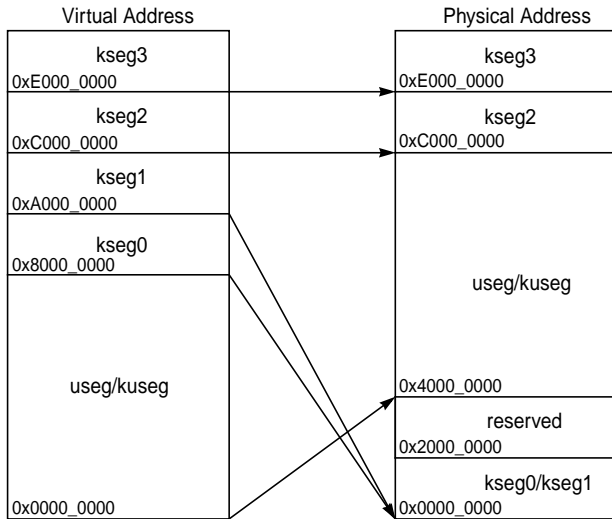


Figure 9 FMT Memory Map (ERL=0) in the 24Kc™ Core

When ERL=1, useg and kuseg become unmapped (virtual address is identical to the physical address) and uncached. This behavior is the same as if there was a TLB. This mapping is shown in Figure 10.

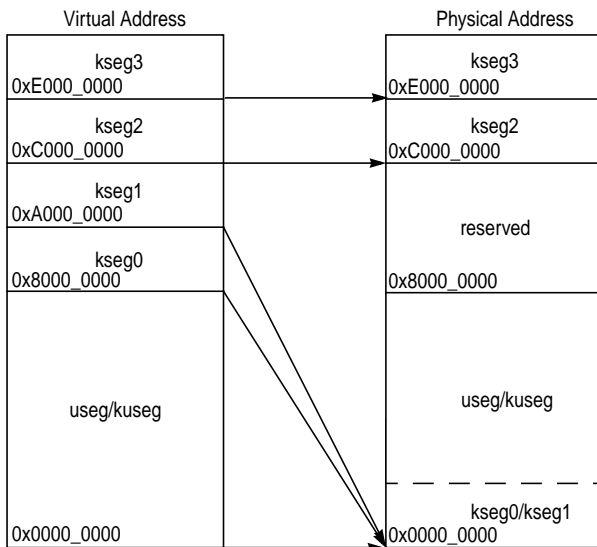


Figure 10 FMT Memory Map (ERL=1) in the 24Kc™ Core

## Instruction Cache

The instruction cache is an on-chip memory block of 16/32/64 KB, with 4-way associativity. Because the instruction cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access rather than having to wait for the physical

address translation. A tag entry holds 20 bits of physical address, a valid bit, a lock bit, and an optional parity bit per way. The instruction data entry holds two instructions (64 bits) per way, as well as 6 bits of pre-decode information to speed the decode of branch and jump instructions, and 9 optional parity bits (one per data byte plus one more for the pre-decode information). The LRU replacement bits (6b) are stored in a separate array.

The instruction cache block also contains and manages the instruction line fill buffer. Besides accumulating data to be written to the cache, instruction fetches that reference data in the line fill buffer are serviced either by a bypass of that data, or data coming from the external interface. The instruction cache control logic controls the bypass function.

The 24Kc core supports instruction-cache locking. Cache locking allows critical code or data segments to be locked into the cache on a “per-line” basis, enabling the system programmer to maximize the efficiency of the system cache.

The cache-locking function is always available on all instruction-cache entries. Entries can then be marked as locked or unlocked on a per entry basis using the CACHE instruction.

## Data Cache

The data cache is an on-chip memory block of 0/16/32/64 KB, with 4-way associativity. Since the data cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access. A tag entry holds 20 bits of physical address, a valid bit, a lock bit, and an optional parity bit per way. The data entry holds 64 bits of data per way, with optional parity per byte. There is an additional array holding dirty bits and LRU replacement algorithm bits (6b LRU, 4b dirty, and optionally 4b dirty parity).

Using 4KB pages in the TLB and 32 or 64KB cache sizes it is possible to get virtual aliasing. A single physical address can exist in multiple cache locations if it was accessed via different virtual addresses. For a 32KB data cache, there is an implementation option to eliminate virtual aliasing. If this option is not selected, or a 64KB cache is implemented, software must take care of any aliasing issues by using a page coloring scheme or some other mechanism.

In addition to instruction-cache locking, the 24Kc core also supports a data-cache locking mechanism identical to the

instruction cache. Critical data segments are locked into the cache on a “per-line” basis. The locked contents can be updated on a store hit, but will not be selected for replacement on a cache miss.

The cache-locking function is always available on all data cache entries. Entries can then be marked as locked or unlocked on a per-entry basis using the CACHE instruction.

## Cache Memory Configuration

The 24Kc core incorporates on-chip instruction and data caches that are usually implemented from readily available single-port synchronous SRAMs and accessed in two cycles: one cycle for the actual SRAM read and another cycle for the tag comparison, hit determination, and way selection. The instruction and data caches each have their own 64-bit data paths and can be accessed simultaneously. Table 9 lists the 24Kc core instruction and data cache attributes.

Table 9 24Kc™ Core Instruction and Data Cache Attributes

Parameter	Instruction	Data
Size	16, 32, or 64 KB*	0, 16, 32, or 64 KB
Organization	4 way set associative	4 way set associative
Line Size	32 Bytes*	32 Bytes
Read Unit	64 bits*	64 bits
Write Policies	N/A	write-through without write allocate, write-back with write allocate
Miss restart after transfer of	miss word	miss word
Cache Locking	per line	per line

\*Logical size of instruction cache. Cache physically contains some extra bits used for precoding the instruction type.

Table 10 OCP Performance Report

Core name	24Kc
-----------	------

## Cache Protocols

The 24Kc core supports the following cache protocols:

- **Uncached:** Addresses in a memory area indicated as uncached are not read from the cache. Stores to such addresses are written directly to main memory, without changing cache contents.
- **Write-through, no write allocate:** Loads and instruction fetches first search the cache, reading main memory only if the desired data does not reside in the cache. On data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents are updated, and main memory is also written. If the cache look-up misses, only main memory is written.
- **Write-back, write allocate:** Stores that miss in the cache will cause a cache refill. Store data, however, is only written to the cache. Caches lines that are written by stores will be marked as dirty. If a dirty line is selected for replacement, the cache line will be written back to main memory.
- **Uncached Accelerated:** Like uncached, data is never loaded into the cache. Store data can be gathered in a write buffer before being sent out on the bus as a bursted write. This is more efficient than sending out individual writes as occurs in regular uncached mode.

## Bus Interface (BIU)

The Bus Interface Unit (BIU) controls the external interface signals. The primary interface implements the Open Core Protocol (OCP). Additionally, the BIU includes a write buffer.

## OCP Interface

Table 10 shows the OCP Performance Report for the 24Kc core. This table lists characteristics about the core and the specific OCP functionality that is supported.



Table 10 OCP Performance Report

Core Identity	TBD
Vendor Code	TBD
Core Code	0x93, visible in ProcessorID field of CP0 <i>PrID</i> register
Revision Code	Visible in Revision field of <i>PrID</i> register
Process dependent	No
Frequency range for this core	Synthesizable, so varies based on process, libraries, and implementation
Area	Synthesizable, so varies based on process, libraries, and implementation
Power Estimate	Synthesizable, so varies based on process, libraries, and implementation
Special reset requirements	No
Number of Interfaces	1 OCP master, 2 OCP slave (DMA access for SPRAMs)
Interface Information:	
• Name	OCPMasterInterface
• Type	Master
<b>Master OCP Interface</b>	
a. Operations issued	RD, WR
b. Issue rate (per OCP cycle)	One per cycle, for all of the types listed above except for a non-standard RD (SYNC) which depends on ack latency.
Maximum number of operations outstanding	6 read operations. All writes are posted, so the OCP fabric determines the maximum number of outstanding writes.
Burst support and effect on issue rates	Fixed burst length of four 64b beats with single request per burst. Burst sequences of WRAP or XOR supported.
High level flow control	None
Number of tags supported and use of those tags	Total of 8 tags: 6 tags for outstanding RD's, 1 tag for WR & 1 tag for SYNC
Connection ID and use of connection information	None
Use of sideband signals	None
Implementation restrictions	<p>1. MReqInfo handled in a user defined way. 3 bits used to send cacheable attribute information or encode type of L2 CACHE instruction, 1 bit used to signify SYNC.</p> <p>2. MAddrSpace is used (2 bits) to indicate L2/L3 access.</p> <p>4. Core clock is synchronous but a multiple of the OCP clock. The ratios supported are 1:1, 1:1.5, 1:2, 1:2.5, 1:3, 1:3.5, 1:4 and 1:5. A helper pulse is required by the core to transfer data from/to the OCP interface without any hazards.</p>
Interface Information:	
• Name	OCPSlaveInterface
• Type	Slave
<b>Slave OCP Interfaces (DMA interface to scratchpad)</b>	

Table 10 OCP Performance Report

a. Operations accepted	RD, WR
b. Issue rate (per OCP cycle)	One per cycle, for all of the types listed above except for a non-standard RD (SYNC) which is not supported.
Maximum number of operations outstanding	2 outstanding operations which includes both RD & WR.
Burst support	Burst access is not supported
High level flow control	Back pressure from slave on data and command accept. Slave assumes no back pressure from the master.
Number of tags supported and use of those tags	Total of 8 tags. Any tag number can be used for read and write operation.
Connection ID and use of connection information	None
Use of sideband signals	None
Implementation restrictions	The slave interface operates at the same clock ratio as that of the master OCP interface.

### Write Buffer

The BIU contains a merging write buffer. The purpose of this buffer is to store and combine write transactions before issuing them to the external interface. The write buffer is organized as four 32-byte buffers. Each buffer contains data from a single 32-byte aligned block of memory.

### Write Through

When using the write-through cache policy, the write buffer significantly reduces the number of write transactions on the external interface and reduces the amount of stalling in the core due to issuance of multiple writes in a short period of time.

### Write Back

The write buffer also holds eviction data for write-back lines. The load-store unit opportunistically pulls dirty data from the cache and sends it to the BIU. It is gathered in the write buffer and sent out as a bursted write.

### Uncached Accelerated

For uncached accelerated references, the write buffer can gather multiple writes together and then perform a bursted write to increase the efficiency of the bus. Uncached accelerated gathering is supported for word and double word stores only.

Gathering of uncached accelerated stores will start on cache-line aligned addresses, i.e. 32 byte aligned addresses. Uncached accelerated word or double word stores that do not meet the conditions required to start gathering will be treated like regular uncached stores.

Once an uncached accelerated store meets the requirements needed to start gathering, a gather buffer is reserved for this store. All subsequent uncached accelerated word or double word stores to the same 32B region will write sequentially into this buffer, independent of the word address associated with these latter stores. The uncached accelerated buffer is tagged with the address of the first store.

An uncached accelerated buffer is written to memory (flushed) if:

1. The last word in the 32-byte entry being gathered is written. (Implicit flush).
2. A PREF Nudge which matches the address associated with the gather buffer (Explicit flush).
3. A SYNC instruction is executed. (Explicit flush).
4. Bits <31:5> of the address of a Load instruction match the address associated with the gather buffer. (Implicit flush)
5. Bits <31:5> of the address of an uncached accelerated store do not match the address associated with the gather buffer. Uncached accelerated store to a different 32B region (Implicit flush)
6. An exception occurs. (Implicit flush)

When an uncached accelerated buffer is flushed, the address sent out on the system interface is the address associated with the gather buffer.

**Caveats:**

- Any uncached loads or stores to unrelated addresses that occur between uncached accelerated stores that are part of a gather sequence will go out of order. They will not enforce ordering.
- One constraint imposed on the gathering is that doubleword stores are only allowed to write to double word aligned locations in the buffer. For example if uncached accelerated gathering starts with a Store Word (SW/SWC1), it may not be followed by a Store Double (SDC1)
- Uncached accelerated stores of the following types are not intended to be used by software and may generate unpredictable results:
  - Byte, Half, or unaligned Stores
  - Store conditionals
- In order for software to be able to run functionally correct on implementations without uncached accelerated stores, software should always generate accesses starting on a cache-line aligned address, proceed to generate correctly incremented sequential addresses and observe the restrictions for uncached accelerated stores.

**Burst Order**

The core is capable of generating burst transactions on the OCP interface. A burst transaction is used to transfer multiple related data items. Burst transactions on the 24Kc core always consist of a single request, followed by four beats of data transfer.

Burst read transactions initiated by the core always contain four 64b data transfers. In addition, the data requested is always a 32-byte-aligned block. Burst reads are always initiated for cacheable instruction or data reads which have missed in the primary instruction or data cache.

The order of words within this 32-byte block varies depending on which of the words in the block is being requested by the execution unit and the ordering protocol selected. The burst always starts with the critical word requested by the execution unit and proceeds in either an ascending or descending order wrapping at the end of an aligned block.

The burst order sequence may be sequential or sub-block. These are equivalent to WRAP and XOR as defined by the OCP protocol. The selection is determined by the static input pin, *SI\_SBlock*.

Table 11 and Table 12 show the implied sequence of address bits 3 and 4 for the two possible burst orders. Since there is only a single request command for a burst sequence, note that only the starting address is actually transmitted by the core.

Table 11 Sequential Burst Order

Starting Address OC_MAddr[4:3]	Address Progression of OC_MAddr[4:3]
00	00, 01, 10, 11
01	01, 10, 11, 00
10	10, 11, 00, 01
11	11, 00, 01, 10

Table 12 Sub-block Burst Order

Starting Address OC_MAddr[4:3]	Address Progression of OC_MAddr[4:3]
00	00, 01, 10, 11
01	01, 00, 11, 10
10	10, 11, 00, 01
11	11, 10, 01, 00

Burst write transactions can also occur when a full 32-byte block is written to memory. This may occur in the case of a cache line eviction, or when a full line has been gathered in the write buffer. For writes, the burst sequence always starts with an initial address of 00 on *OC\_MAddr[4:3]*, so the write burst sequence is actually the same for sequential or sub-block orders.

**SimpleBE Mode**

To aid in attaching the 24Kc core to structures which cannot easily handle arbitrary byte enable patterns, there is a mode that generates only “simple” byte enables. Only byte enables representing naturally aligned byte, halfword, word, and doubleword transactions will be generated. Legal byte enable patterns are shown in Table 13.

Table 13 Valid SimpleBE Byte Enable Patterns

OC_MByteEn[7:0] or OC_MDataByteEn[7:0]
0000_0001
0000_0010
0000_0100
0000_1000
0001_0000
0010_0000
0100_0000
1000_0000
0000_0011
0000_1100
0011_0000
1100_0000
0000_1111
1111_0000
1111_1111

The only case where a read can generate “non-simple” byte enables is on an uncached tri-byte load (LWL/LWR). In SimpleBE mode, such reads will be converted into a word read on the external interface.

Writes with non-simple byte enable patterns can arise when a sequence of stores is processed by the merging write buffer, or from uncached tri-byte stores (SWL/SWR). In SimpleBE mode, these stores will be broken into multiple write transactions.

### Clocking

The core has 3 primary clock domains:

- Core domain - This is the main core clock domain, controlled by the *SI\_ClkIn* clock input.
- OCP domain - This domain controls the OCP bus interface logic. This domain is synchronous to *SI\_ClkIn*, but can be run at lower frequencies. Core to bus ratios of 1:1, 3:2, 2:1, 5:2, 3:1, 7:2, 4:1 and 5:1 are supported. The core does not contain an explicit OCP input clock; all flops are actually controlled by *SI\_ClkIn*. To enable the core to determine the frequency and phase relationship between the core and OCP domains, a “helper” pulse, *SI\_OCPSync*, is required in the *SI\_ClkIn* domain. *SI\_OCPSync* is used internally to control when to drive OCP outputs and when to sample OCP inputs. Figure 11 illustrates the required waveform for *SI\_OCPSync* at the various clock ratios. All OCP outputs are registered. All OCP inputs except *OC\_SCmdAccept* and *OC\_SDataAccept* are also registered.
- TAP domain - This is a low speed clock domain for the EJTAG TAP controller, controlled by the *EJ\_TCK* pin. It is asynchronous to *SI\_ClkIn*.

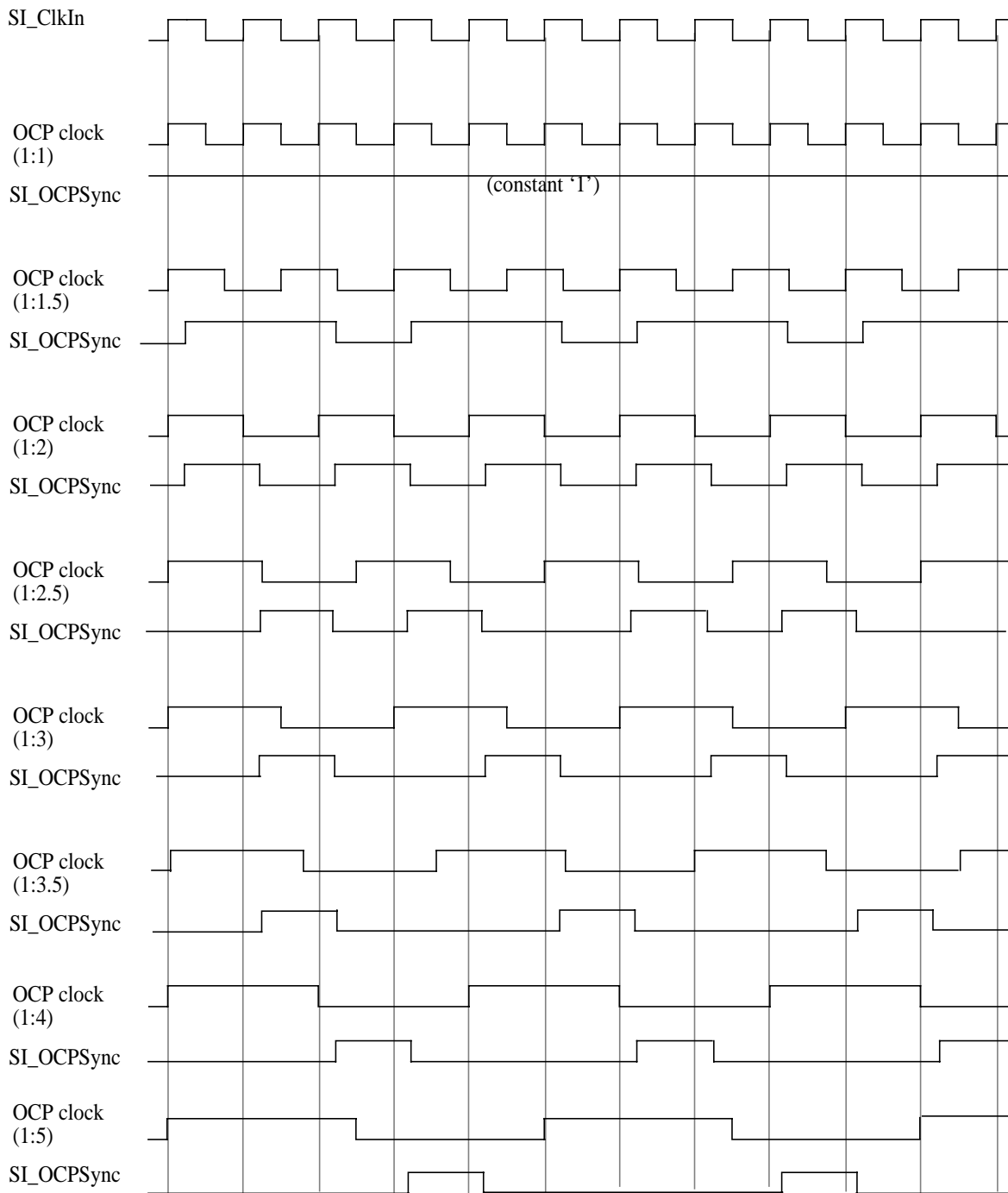


Figure 11 Required *SI\_OCPSync* waveforms

### Hardware Reset

Unlike previous MIPS cores, a 24Kc core only has a single reset input. Historically, cold reset was used to reset a PLL.

In synthesizable cores without a PLL, the two inputs were ORed together internally and then treated identically (except for a *Status* bit indicating which reset was seen).

The 24Kc interface has removed the second reset type and only includes the *SI\_Reset* pin.

The *SI\_Reset* input is used to initialize critical hardware state. It can be asserted either synchronously or asynchronously to the core clock, *SI\_ClkIn*, and will trigger a Reset exception. The reset signal is active high, and must be asserted for a minimum of 5 *SI\_ClkIn* cycles. The falling edge triggers the Reset exception. The reset signal must be asserted at power-on or whenever hardware initialization of the core is desired.

In debug mode, EJTAG can request that a ‘soft’ reset be masked. This request is signalled via the *EJ\_SRstE* pin. When this pin is deasserted, the system can choose to block some sources of soft reset. Hard resets, such as power-on reset or a reset switch should not be blocked by this signal.

## Power Management

The 24Kc core offers a number of power management features, including low-power design, active power management, and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

The 24Kc core provides two mechanisms for system-level low power support:

- Register-controlled power management
- Instruction-controlled power management

### Register-Controlled Power Management

The RP bit in the CP0 Status register provides a software mechanism for placing the system into a low power state. The state of the RP bit is available externally via the *SI\_RP* signal. The external agent then decides whether to place the device in a low power mode, such as reducing the system clock frequency.

Three additional bits, *Status\_EXL*, *Status\_ERL*, and *Debug\_DM* support the power management function by allowing the user to change the power state if an exception or error occurs while the 24Kc core is in a low power state. Depending on what type of exception is taken, one of these three bits will be asserted and reflected on the *SI\_EXL*, *SI\_ERL*, or *EJ\_DebugM* outputs. The external agent can look at these signals and determine whether to leave the low power state to service the exception.

The following 4 power-down signals are part of the system interface and change state as the corresponding bits in the CP0 registers are set or cleared:

- The *SI\_RP* signal represents the state of the RP bit (27) in the CP0 *Status* register.
- The *SI\_EXL* signal represents the state of the EXL bit (1) in the CP0 *Status* register.
- The *SI\_ERL* signal represents the state of the ERL bit (2) in the CP0 *Status* register.
- The *EJ\_DebugM* signal represents the state of the DM bit (30) in the CP0 *Debug* register.

### Instruction-Controlled Power Management

The second mechanism for invoking power-down mode is through execution of the WAIT instruction. When the WAIT instruction is executed, the internal clock is suspended; however, the internal timer and some of the input pins (*SI\_Int[5:0]*, *SI\_NMI*, and *SI\_Reset*) continue to run. Once the CPU is in instruction-controlled power management mode, any interrupt, NMI, or reset condition causes the CPU to exit this mode and resume normal operation.

The 24Kc core asserts the *SI\_Sleep* signal, which is part of the system interface, whenever the WAIT instruction is executed. The assertion of *SI\_Sleep* indicates that the clock has stopped and the 24Kc core is waiting for an interrupt.

### Local clock gating

A majority of the power consumed by the 24Kc core is often in the clock tree and clocking registers. The core has support for extensive use of local gated-clocks. Power-conscious implementors can use these gated clocks to significantly reduce power consumption within the core.

### CorExtend™ User Defined Instruction Extensions

The optional CorExtend User Defined Instruction (UDI) block enables the implementation of a small number of application-specific instructions that are tightly coupled to the core’s integer execution unit.

The interface to the CorExtend block is similar to the Multiply-Divide Unit, allowing non-blocking, pipelined multi-cycle operations. A portion of the hooks into the MDU control logic and also allows the HI/LO accumulation registers to be used by the CorExtend block.

CorExtend instructions may operate on a general-purpose register, immediate data specified by the instruction word, or local state stored within the UDI block. The destination may be a general-purpose register, HI/LO, or local UDI state. The operation may complete in one cycle or multiple cycles, if desired.

## Coprocessor 2 interface

The 24Kc core can be configured to have an interface for an on-chip coprocessor. The interface allows the coprocessor to be tightly coupled to the processor core, allowing high performance solutions, like integrating a graphics accelerator or custom DSP.

The coprocessor interface is extensible and standardized on MIPS cores, allowing design reuse. The 24Kc core supports a subset of the full coprocessor interface standard: single issue, 64 bit in-order data transfers.

The coprocessor interface is designed to ease integration with customer IP. The interface allows high-performance communication between the core and coprocessor. There are no late or critical timing signals on the interface.

## Data Scratchpad RAM (DSPRAM)

The 24Kc core can be configured to include an optional Data scratchpad RAM independent of the data cache configuration. A separate OCP slave interface allows a DMA master to access the data scratchpad RAM.

To demonstrate use of the scratchpad capability, MIPS provides a default design that includes one contiguous 8KB RAM with cache like access. DSPRAM hit supersedes data cache hit. DSPRAM is indexed by virtual address. The hit information is based on the physical address in the base register. DSPRAM can be mapped to either cacheable or non-cacheable address space. A sophisticated arbitration scheme and instruction slip in the pipe prevents unnecessary stalls.

Only store instructions which are guaranteed to complete and hit in the DSPRAM, arbitrate for the RAM. The DMA access priority with respect to the core access is determined by the input pin *SI\_DMA\_Priority*. The DSPRAM interface supports multi-cycle access to the RAM array to accommodate slow devices or larger memory sizes. The interface allows addressing of DSPRAM sizes up to 1MB. The interface also supports 64-bit wide data access and provides a mechanism to back-stall the core pipeline.

## Instruction Scratchpad RAM (ISPRAM)

The 24Kc core can be configured to include an optional instruction scratchpad RAM independent of the instruction cache configuration. A separate OCP slave interface allows a DMA master to access the instruction scratchpad RAM.

To demonstrate use of the scratchpad capability, MIPS provides a default design that includes one contiguous 8KB RAM with cache like access. ISPRAM hit supersedes instruction cache hit. ISPRAM is indexed by virtual address. The hit information is based on the physical address in the base register. ISPRAM can be mapped to either cacheable or non-cacheable address space.

The DMA access priority with respect to the core access is determined by the input pin *SI\_IDMA\_Priority*. The ISPRAM interface supports multi-cycle access to the RAM array to accommodate slow devices or larger memory sizes. The interface allows addressing of ISPRAM sizes up to 1MB. The interface also supports 64-bit wide data access and provides a mechanism to back-stall the core pipeline.

## EJTAG Debug Support

The 24Kc core includes an Enhanced JTAG (EJTAG) block for use in the software debug of application and kernel code. In addition to standard user/supervisor/kernel modes of operation, the 24Kc core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a debug exception return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

Refer to the section called "[External Interface Signals](#)" on [page 32](#) for a list of EJTAG interface signals.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the 24Kc core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define what registers are selected and how they are used.

## Debug Registers

Three debug registers (*DEBUG*, *DEPC*, and *DESAVE*) have been added to the MIPS Coprocessor 0 (CP0) register set. The *DEBUG* register shows the cause of the debug exception and is used for setting up single-step operations. The *DEPC*, or Debug Exception Program Counter, register

holds the address on which the debug exception was taken. This is used to resume program execution after the debug operation finishes. Finally, the *DESAVE*, or Debug Exception Save, register enables the saving of general-purpose registers used during execution of the debug exception handler.

To exit debug mode, a Debug Exception Return (DERET) instruction is executed. When this instruction is executed, the system exits debug mode, allowing normal execution of application and system code to resume.

### **EJTAG Hardware Breakpoints**

There are several types of simple hardware breakpoints defined in the EJTAG specification. These breakpoints stop the normal operation of the CPU and force the system into debug mode. There are two types of simple hardware breakpoints implemented in the 24Kc core: Instruction breakpoints and Data breakpoints.

During synthesis, the 24Kc core can be configured with or without hardware breakpoints. The following breakpoint options are supported:

- Zero or four instruction breakpoints
- Zero or two data breakpoints

Instruction breaks occur on instruction fetch operations, and the break is set on the virtual address. Instruction breaks can also be made on the ASID value used by the MMU. A mask can be applied to the virtual address to set breakpoints on a range of instructions.

Data breakpoints occur on load/store transactions. Breakpoints are set on virtual address and ASID values, similar to the Instruction breakpoint. Data breakpoints can be set on a load, a store, or both. Data breakpoints can also be set based on the value of the load/store operation. Finally, masks can be applied to both the virtual address and the load/store value.

### **MIPS Trace**

The 24Kc core includes optional MIPS Trace support for real-time tracing of instruction addresses, data addresses and data values. The trace information is collected in an on-chip or off-chip memory, for post-capture processing by trace regeneration software.

On-chip trace memory may be configured in size from 0 to 8 MB; it is accessed through the existing EJTAG TAP interface and requires no additional chip pins. Off-chip

trace memory is accessed through a special trace probe and can be configured to use 4, 8, or 16 data pins plus a clock.

### **Testability**

Testability for production testing of the core is supported through the use of internal scan and memory BIST.

### **Internal Scan**

Full mux-based scan for maximum test coverage is supported, with a configurable number of scan chains. ATPG test coverage can exceed 99%, depending on standard cell libraries and configuration options.

### **Memory BIST**

Memory BIST for the cache arrays, scratchpad memories and on-chip trace memory is optional, but can be implemented either through the use of integrated BIST features provided with the core, or inserted with an industry-standard memory BIST CAD tool.

### **Integrated Memory BIST**

The core provides an integrated memory BIST solution for testing the internal cache SRAMs, scratchpad RAMs and on-chip trace RAM, using BIST controllers and logic tightly coupled to the cache subsystem. Several parameters associated with the integrated BIST controllers are configurable, including the algorithm (March C+ or IFA-13).

### **User-specified Memory BIST**

Memory BIST can also be inserted with a CAD tool or other user-specified method. Wrapper modules and signal buses of configurable width are provided within the core to facilitate this approach.

### **Build-Time Configuration Options**

The 24Kc core allows a number of features to be customized based on the intended application. [Table 14](#) summarizes the key configuration options that can be selected when the core is synthesized and implemented.



For a core that has already been built, software can determine the value of many of these options by querying an appropriate register field. Refer to the *MIPS32 24K Processor Core Family Software User's Manual* for a more

complete description of these fields. The value of some options that do not have a functional effect on the core are not visible to software.

Table 14 Build-time Configuration Options

Option	Choices	Software Visibility
Integer register file sets	1, 2, or 4	SRSCtl <sub>HSS</sub>
Integer register file implementation style	Flops or generator	N/A
Memory Management Type	TLB or FMT	Config <sub>MT</sub>
TLB Size	16, 32, or 64 dual entries	Config <sub>1MMUSize</sub>
TLB data array implementation style	Flops or generator	N/A
Instruction hardware breakpoints	0 or 4	DCR <sub>IB</sub> , IBS <sub>BCN</sub>
Data hardware breakpoints	0 or 2	DCR <sub>DB</sub> , DBS <sub>BCN</sub>
MIPS Trace support	Present or not	Config <sub>3TL</sub>
MIPS Trace memory location	On-core, off-chip or both	TCBCONFIG <sub>OnT</sub> , TCBCONFIG <sub>OfT</sub>
MIPS Trace on-chip memory size	256B - 8MB	TCBCONFIG <sub>SZ</sub>
MIPS Trace triggers	0 - 8	TCBCONFIG <sub>TRIG</sub>
CorExtend interface (Pro only)	Present or not	Config <sub>UDI</sub> *
Coprocessor2 interface	Present or not	Config <sub>1C2</sub> *
Instruction ScratchPad RAM interface	Present or not	Config <sub>ISP</sub> *
Data ScratchPad RAM interface	Present or not	Config <sub>DSP</sub> *
I-cache size	16, 32, or 64 KB	Config <sub>1IS</sub>
D-cache size	0, 16, 32, or 64 KB	Config <sub>1DL</sub> , Config <sub>1DS</sub>
D-cache hardware aliasing support	Present or not (for 32KB only)	Config <sub>7AR</sub>
Cache parity	Present or not	ErrCtl <sub>PE</sub>
Memory BIST	Integrated (March C+ or March C+ plus IFA-13), custom, or none	N/A
Clock gating	Top-level, integer register file array, TLB array, fine-grain, or none	N/A

\* These bits indicate the presence of an external block. Bits will not be set if interface is present, but block is not.

## Instruction Set

The 24Kc core instruction set complies with the MIPS32 instruction set architecture. Table 15 provides a summary of instructions implemented by the 24Kc core.

Table 15 24Kc™ Core Instruction Set

Instruction	Description	Function
ADD	Integer Add	$Rd = Rs + Rt$
ADDI	Integer Add Immediate	$Rt = Rs + Immed$
ADDIU	Unsigned Integer Add Immediate	$Rt = Rs +_U Immed$
ADDIUPC	Unsigned Integer Add Immediate to PC (MIPS16 only)	$Rt = PC +_U Immed$
ADDU	Unsigned Integer Add	$Rd = Rs +_U Rt$
AND	Logical AND	$Rd = Rs \& Rt$
ANDI	Logical AND Immediate	$Rt = Rs \& (0_{16}    Immed)$
ASMACRO	Application Specific Macro - allows macro sequences to be defined by implementor (MIPS16 only)	Defined by implementor
B	Unconditional Branch (Assembler idiom for: BEQ r0, r0, offset)	$PC += (int)offset$
BAL	Branch and Link (Assembler idiom for: BGEZAL r0, offset)	$GPR[31] = PC + 8$ $PC += (int)offset$
BC2F	Branch On COP2 Condition False	if COP2Condition(cc) == 0 PC += (int)offset
BC2FL	Branch On COP2 Condition False Likely	if COP2Condition(cc) == 0 PC += (int)offset else Ignore Next Instruction
BC2T	Branch On COP2 Condition True	if COP2Condition(cc) == 1 PC += (int)offset
BC2TL	Branch On COP2 Condition True Likely	if COP2Condition(cc) == 1 PC += (int)offset else Ignore Next Instruction
BEQ	Branch On Equal	if $Rs == Rt$ PC += (int)offset
BEQL	Branch On Equal Likely	if $Rs == Rt$ PC += (int)offset else Ignore Next Instruction
BGEZ	Branch on Greater Than or Equal To Zero	if ! $Rs[31]$ PC += (int)offset
BGEZAL	Branch on Greater Than or Equal To Zero And Link	$GPR[31] = PC + 8$ if ! $Rs[31]$ PC += (int)offset
BGEZALL	Branch on Greater Than or Equal To Zero And Link Likely	$GPR[31] = PC + 8$ if ! $Rs[31]$ PC += (int)offset else Ignore Next Instruction

Table 15 24Kc™ Core Instruction Set (Continued)

Instruction	Description	Function
BGEZL	Branch on Greater Than or Equal To Zero Likely	if !Rs[31] PC += (int)offset else Ignore Next Instruction
BGTZ	Branch on Greater Than Zero	if !Rs[31] && Rs != 0 PC += (int)offset
BGTZL	Branch on Greater Than Zero Likely	if !Rs[31] && Rs != 0 PC += (int)offset else Ignore Next Instruction
BLEZ	Branch on Less Than or Equal to Zero	if Rs[31]    Rs == 0 PC += (int)offset
BLEZL	Branch on Less Than or Equal to Zero Likely	if Rs[31]    Rs == 0 PC += (int)offset else Ignore Next Instruction
BLTZ	Branch on Less Than Zero	if Rs[31] PC += (int)offset
BLTZAL	Branch on Less Than Zero And Link	GPR[31] = PC + 8 if Rs[31] PC += (int)offset
BLTZALL	Branch on Less Than Zero And Link Likely	GPR[31] = PC + 8 if Rs[31] PC += (int)offset else Ignore Next Instruction
BLTZL	Branch on Less Than Zero Likely	if Rs[31] PC += (int)offset else Ignore Next Instruction
BNE	Branch on Not Equal	if Rs != Rt PC += (int)offset
BNEL	Branch on Not Equal Likely	if Rs != Rt PC += (int)offset else Ignore Next Instruction
BREAK	Breakpoint	Break Exception
CACHE	Cache Operation	See Software User's Manual
CFC2	Move Control Word From Coprocessor 2	Rt = CCR[2, Rs]
CLO	Count Leading Ones	Rd = NumLeadingOnes(Rs)
CLZ	Count Leading Zeroes	Rd = NumLeadingZeroes(Rs)
COP0	Coprocessor 0 Operation	See Software User's Manual
COP2	Coprocessor 2 Operation	See Coprocessor 2 Description
CTC2	Move Control Word To Coprocessor 2	CCR[2, n] = Rt

Table 15 24Kc™ Core Instruction Set (Continued)

Instruction	Description	Function
DERET	Return from Debug Exception	PC = DEPC Exit Debug Mode
DI	Atomically Disable Interrupts	Rt = Status; Status <sub>IE</sub> = 0
DIV	Divide	LO = (int)Rs / (int)Rt HI = (int)Rs % (int)Rt
DIVU	Unsigned Divide	LO = (uns)Rs / (uns)Rt HI = (uns)Rs % (uns)Rt
EHB	Execution Hazard Barrier	Stop instruction execution until execution hazards are cleared
EI	Atomically Enable Interrupts	Rt = Status; Status <sub>IE</sub> = 1
ERET	Return from Exception	if SR[2] PC = ErrorEPC else PC = EPC SR[1] = 0 SR[2] = 0 LL = 0
EXT	Extract Bit Field	Rt = ExtractField(Rs, pos, size)
INS	Insert Bit Field	Rt = InsertField(Rs, Rt, pos, size)
J	Unconditional Jump	PC = PC[31:28]    offset<<2
JAL	Jump and Link	GPR[31] = PC + 8 PC = PC[31:28]    offset<<2
JALR	Jump and Link Register	Rd = PC + 8 PC = Rs
JALR.HB	Jump and Link Register with Hazard Barrier	Like JALR, but also clears execution and instruction hazards
JALRC	Jump and Link Register Compact - do not execute instruction in jump delay slot(MIPS16 only)	Rd = PC + 2 PC = Rs
JR	Jump Register	PC = Rs
JR.HB	Jump Register with Hazard Barrier	Like JR, but also clears execution and instruction hazards
JRC	Jump Register Compact - do not execute instruction in jump delay slot (MIPS16 only)	PC = Rs
LB	Load Byte	Rt = (byte)Mem[Rs+offset]
LBU	Unsigned Load Byte	Rt = (ubyte)Mem[Rs+offset]
LDC2	Load Doubleword to Coprocessor 2	CPR[2, Rt] = Mem[Rs+offset]
LH	Load Halfword	Rt = (half)Mem[Rs+offset]

Table 15 24Kc™ Core Instruction Set (Continued)

Instruction	Description	Function
LHU	Unsigned Load Halfword	$Rt = (\text{uhalf})\text{Mem}[\text{Rs}+\text{offset}]$
LL	Load Linked Word	$Rt = \text{Mem}[\text{Rs}+\text{offset}]$ LL = 1 LLAdr = Rs + offset
LUI	Load Upper Immediate	$Rt = \text{immediate} \ll 16$
LW	Load Word	$Rt = \text{Mem}[\text{Rs}+\text{offset}]$
LWC2	Load Word To Coprocessor 2	$\text{CPR}[2, Rt] = (\text{word})\text{Mem}[\text{Rs}+\text{offset}]$
LWPC	Load Word, PC relative	$Rt = \text{Mem}[\text{PC}+\text{offset}]$
LWL	Load Word Left	See Architecture Reference Manual
LWR	Load Word Right	See Architecture Reference Manual
MADD	Multiply-Add	HI   LO += (int)Rs * (int)Rt
MADDU	Multiply-Add Unsigned	HI   LO += (uns)Rs * (uns)Rt
MFC0	Move From Coprocessor 0	$Rt = \text{CPR}[0, Rd, sel]$
MFC2	Move From Coprocessor 2	$Rt = \text{CPR}[2, Rd, sel]$
MFHC2	Move From High Half of Coprocessor 2	$Rt = \text{CPR}[2, Rd, sel]_{63..32}$
MFHI	Move From HI	Rd = HI
MFLO	Move From LO	Rd = LO
MOVN	GPR Conditional Move on Not Zero	if Rt ≠ 0 then Rd = Rs
MOVZ	GPR Conditional Move on Zero	if Rt = 0 then Rd = Rs
MSUB	Multiply-Subtract	HI   LO -= (int)Rs * (int)Rt
MSUBU	Multiply-Subtract Unsigned	HI   LO -= (uns)Rs * (uns)Rt
MTC0	Move To Coprocessor 0	$\text{CPR}[0, n, Sel] = Rt$
MTC2	Move To Coprocessor 2	$\text{CPR}[2, n, sel] = Rt$
MTHC2	Move To High Half of Coprocessor 2	$\text{CPR}[2, Rd, sel] = Rt \   $ $\text{CPR}[2, Rd, sel]_{31..0}$
MTHI	Move To HI	HI = Rs
MTLO	Move To LO	LO = Rs
MUL	Multiply with register write	HI   LO =Unpredictable $Rd = ((\text{int})Rs * (\text{int})Rt)_{31..0}$
MULT	Integer Multiply	HI   LO = (int)Rs * (int)Rd
MULTU	Unsigned Multiply	HI   LO = (uns)Rs * (uns)Rd

Table 15 24Kc™ Core Instruction Set (Continued)

Instruction	Description	Function
NOP	No Operation (Assembler idiom for: SLL r0, r0, r0)	
NOR	Logical NOR	$Rd = \sim(Rs \mid Rt)$
OR	Logical OR	$Rd = Rs \mid Rt$
ORI	Logical OR Immediate	$Rt = Rs \mid Immed$
PREF	Prefetch	Load Specified Line into Cache
RDHWR	Read Hardware Register	Allows unprivileged access to registers enabled by HWREna register
RDPGPR	Read GPR from Previous Shadow Set	$Rt = SGPR[SRSCtl_{PSS}, Rd]$
RESTORE	Restore registers and deallocate stack frame (MIPS16 only)	See Architecture Reference Manual
ROTR	Rotate Word Right	$Rd = Rt_{sa-1..0} \parallel Rt_{31..sa}$
ROTRV	Rotate Word Right Variable	$Rd = Rt_{Rs-1..0} \parallel Rt_{31..Rs}$
SAVE	Save registers and allocate stack frame (MIPS16 only)	See Architecture Reference Manual
SB	Store Byte	$(byte)Mem[Rs+offset] = Rt$
SC	Store Conditional Word	if $LL = 1$ $mem[Rs+offset] = Rt$ $Rt = LL$
SDBBP	Software Debug Break Point	Trap to SW Debug Handler
SDC2	Store Doubleword from Coprocessor 2	$Mem[Rs+offset] = CPR[2, Rt]$
SEB	Sign Extend Byte	$Rd = (byte)Rs$
SEH	Sign Extend Half	$Rd = (half)Rs$
SH	Store Half	$(half)Mem[Rs+offset] = Rt$
SLL	Shift Left Logical	$Rd = Rt \ll sa$
SLLV	Shift Left Logical Variable	$Rd = Rt \ll Rs[4:0]$
SLT	Set on Less Than	if $(int)Rs < (int)Rt$ $Rd = 1$ else $Rd = 0$
SLTI	Set on Less Than Immediate	if $(int)Rs < (int)Immed$ $Rt = 1$ else $Rt = 0$
SLTIU	Set on Less Than Immediate Unsigned	if $(uns)Rs < (uns)Immed$ $Rt = 1$ else $Rt = 0$

Table 15 24Kc™ Core Instruction Set (Continued)

Instruction	Description	Function
SLTU	Set on Less Than Unsigned	if (uns)Rs < (uns)Immed Rd = 1 else Rd = 0
SRA	Shift Right Arithmetic	Rd = (int)Rt >> sa
SRAV	Shift Right Arithmetic Variable	Rd = (int)Rt >> Rs[4:0]
SRL	Shift Right Logical	Rd = (uns)Rt >> sa
SRLV	Shift Right Logical Variable	Rd = (uns)Rt >> Rs[4:0]
SSNOP	Superscalar Inhibit No Operation	NOP
SUB	Integer Subtract	Rt = (int)Rs - (int)Rd
SUBU	Unsigned Subtract	Rt = (uns)Rs - (uns)Rd
SW	Store Word	Mem[Rs+offset] = Rt
SWC2	Store Word From Coprocessor 2	Mem[Rs+offset] = CPR[2,Rt] <sub>31..0</sub>
SWL	Store Word Left	See Architecture Reference Manual
SWR	Store Word Right	See Architecture Reference Manual
SYNC	Synchronize	See Software User's Manual
SYNCI	Synchronize Caches to Make Instruction Writes Effective	Fore D-cache writeback and I-cache invalidate on specified address
SYSCALL	System Call	SystemCallException
TEQ	Trap if Equal	if Rs == Rt TrapException
TEQI	Trap if Equal Immediate	if Rs == (int)Immed TrapException
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	if (int)Rs >= (int)Immed TrapException
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	if (uns)Rs >= (uns)Immed TrapException
TGEU	Trap if Greater Than or Equal Unsigned	if (uns)Rs >= (uns)Rt TrapException
TLBWI	Write Indexed TLB Entry	See Software Users Manual
TLBWR	Write Random TLB Entry	See Software Users Manual
TLBP	Probe TLB for Matching Entry	See Software Users Manual
TLBR	Read Index for TLB Entry	See Software Users Manual

Table 15 24Kc™ Core Instruction Set (Continued)

Instruction	Description	Function
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupts	Stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	SGPR[SRSCtl <sub>PSS</sub> , Rd] = Rt
WSBH	Word Swap Bytes Within HalfWords	Rd = Rt <sub>23..16</sub>    Rt <sub>31..24</sub>    Rt <sub>7..0</sub>    Rt <sub>15..8</sub>
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed
ZEB	Zero extend byte (MIPS16 only)	Rt = (ubyte) Rs
ZEH	Zero extend half (MIPS16 only)	Rt = (uhalf) Rs

## External Interface Signals

This section describes the signal interface of the 24Kc microprocessor core.

The pin direction key for the signal descriptions is shown in [Table 16](#) below.

The 24Kc core signals are listed in [Table 17](#) below. Note that the signals are grouped by logical function, not by expected physical location. All signals, with the exception of *EJ\_TRST\_N*, are active-high signals. *EJ\_DINT* and *SI\_NMI* go through edge-detection logic so that only one exception is taken each time they are asserted.

Table 16 24Kc™ Core Signal Direction Key

Dir	Description
I	Input to the 24Kc core sampled on the rising edge of the appropriate CLK signal.
O	Output of the 24Kc core, unless otherwise noted, driven at the rising edge of the appropriate CLK signal.
A	Asynchronous inputs that are synchronized by the core.
S	Static input to the 24Kc core. These signals are normally tied to either power or ground and should not change state while <i>SI_Reset</i> is deasserted.
SO	Static output from the 24Kc core.



Table 17 24Kc™ Core Signal Descriptions

Signal Name	Type	Description																		
<b>System Interface</b>																				
<i>Clock Signals:</i>																				
<i>SI_ClkIn</i>	I	Clock Input.																		
<i>SI_OCPSync</i>	I	<p>Signal indicating phase and frequency relationships between <i>SI_ClkIn</i> and the OCP clock domain. The width of this pulse is related to an <i>SI_ClkIn</i> period.</p> <p>Note that no direct OCP clock input is present on the core. Instead, all bus interface flops are clocked with the high-speed core clock, and the <i>SI_OCPSync</i> signal is used to indicate when inputs are sampled or outputs are enabled. The pattern for various OCP-to-core clock ratios is shown in the table below, assuming the pattern starts from the point where the rising edges of both clocks are aligned:</p> <table border="1"> <thead> <tr> <th>Clock Ratio</th> <th>Sync Pattern</th> </tr> </thead> <tbody> <tr> <td>1:1</td> <td><b>111...</b></td> </tr> <tr> <td>1:1.5</td> <td><b>110110...</b></td> </tr> <tr> <td>1:2</td> <td><b>1010...</b></td> </tr> <tr> <td>1:2.5</td> <td><b>0101001010...</b></td> </tr> <tr> <td>1:3</td> <td><b>010010...</b></td> </tr> <tr> <td>1:3.5</td> <td><b>00100100010010...</b></td> </tr> <tr> <td>1:4</td> <td><b>00100010...</b></td> </tr> <tr> <td>1:5</td> <td><b>0001000010...</b></td> </tr> </tbody> </table>	Clock Ratio	Sync Pattern	1:1	<b>111...</b>	1:1.5	<b>110110...</b>	1:2	<b>1010...</b>	1:2.5	<b>0101001010...</b>	1:3	<b>010010...</b>	1:3.5	<b>00100100010010...</b>	1:4	<b>00100010...</b>	1:5	<b>0001000010...</b>
Clock Ratio	Sync Pattern																			
1:1	<b>111...</b>																			
1:1.5	<b>110110...</b>																			
1:2	<b>1010...</b>																			
1:2.5	<b>0101001010...</b>																			
1:3	<b>010010...</b>																			
1:3.5	<b>00100100010010...</b>																			
1:4	<b>00100010...</b>																			
1:5	<b>0001000010...</b>																			
<i>SI_ClkOut</i>	O	Reference Clock for external use. This clock signal provides a reference for deskewing any clock insertion delay created by the internal clock buffering in the core.																		
<i>Reset Signals:</i>																				
<i>SI_NMI</i>	A	Non-Maskable Interrupt. An edge detect is used on this signal. When this signal is sampled asserted (high) one clock after being sampled deasserted, an NMI is posted to the core.																		
<i>SI_Reset</i>	A	Reset Signal. Causes a Reset Exception in the core.																		
<i>Power Management Signals:</i>																				
<i>SI_ERL</i>	O	This signal represents the state of the ERL bit (2) in the CP0 <i>Status</i> register and indicates the error level. The core asserts <i>SI_ERL</i> whenever a Reset, CacheError, or NMI exception is taken.																		
<i>SI_EXL</i>	O	This signal represents the state of the EXL bit (1) in the CP0 <i>Status</i> register and indicates the exception level. The core asserts <i>SI_EXL</i> whenever any exception other than a Reset, Cache Error, NMI, or Debug exception is taken.																		
<i>SI_RP</i>	O	This signal represents the state of the RP bit (27) in the CP0 <i>Status</i> register. Software can write this bit to indicate that a reduced power mode may be entered.																		
<i>SI_Sleep</i>	O	This signal is asserted by the core whenever the WAIT instruction is executed. The assertion of this signal indicates that the clock has stopped and that the core is waiting for an interrupt.																		
<i>Interrupt Signals:</i>																				
<i>SI_EICPresent</i>	S	Indicates whether an external interrupt controller is present. Value is visible to software in the <i>Config3</i> <sub>VEIC</sub> register field.																		

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description
<i>SI_EISS[3:0]</i>	I	General purpose register shadow set number to be used when servicing an interrupt in EIC interrupt mode.
<i>SI_IAck</i>	O	Interrupt acknowledge indication for use in external interrupt controller mode. This signal is active for a single <i>SI_ClkIn</i> cycle when an interrupt is taken. When the processor initiates the interrupt exception, it loads the value of the <i>SI_Int[5:0]</i> pins into the <i>Cause<sub>R IPL</sub></i> field (overlaid with <i>Cause<sub>IP7..IP2</sub></i> ), and signals the external interrupt controller to notify it that the current interrupt request is being serviced. This allows the controller to advance to another pending higher-priority interrupt, if desired.
<i>SI_Int[5:0]</i>	I/A	<p>Active high Interrupt pins. These signals are driven by external logic and when asserted indicate an interrupt exception to the core. The interpretation of these signals depends on the interrupt mode in which the core is operating; the interrupt mode is selected by software.</p> <p>The <i>SI_Int</i> signals go through synchronization logic and can be asserted asynchronously to <i>SI_ClkIn</i>. In External Interrupt Controller (EIC) mode, however, the interrupt pins are interpreted as an encoded value, so they must be asserted synchronously to <i>SI_ClkIn</i> to guarantee that all bits are received by the core in a particular cycle.</p> <p>The interrupt pins are level sensitive and should remain asserted until the interrupt has been serviced.</p> <p>In Release 1 Interrupt Compatibility mode:</p> <ul style="list-style-type: none"> <li>• All 6 interrupt pins have the same priority as far as the hardware is concerned.</li> <li>• Interrupts are non-vectorized.</li> </ul> <p>In Vectored Interrupt (VI) mode:</p> <ul style="list-style-type: none"> <li>• The <i>SI_Int</i> pins are interpreted as individual hardware interrupt requests.</li> <li>• Internally, the core prioritizes the hardware interrupts and chooses an interrupt vector.</li> </ul> <p>In External Interrupt Controller (EIC) mode:</p> <ul style="list-style-type: none"> <li>• An external block prioritizes its various interrupt requests and produces a vector number of the highest priority interrupt to be serviced.</li> <li>• The vector number is driven on the <i>SI_Int</i> pins, and is treated as a 6-bit encoded value in the range of 0..63.</li> <li>• When the core starts the interrupt exception, signaled by the assertion of <i>SI_IAck</i>, it loads the value of the <i>SI_Int[5:0]</i> pins into the <i>Cause<sub>R IPL</sub></i> field (overlaid with <i>Cause<sub>IP7..IP2</sub></i>). The interrupt controller can then signal another interrupt.</li> </ul>
<i>SI_IPL[5:0]</i>	O	Current interrupt priority level from the <i>Cause<sub>IPL</sub></i> register field, provided for use by an external interrupt controller. This value is updated whenever <i>SI_IAck</i> is asserted.
<i>SI_IPPCI[2:0]</i>	S	Indicates the <i>SI_Int</i> hardware interrupt pin that the performance counter interrupt pin ( <i>SI_PCInt</i> ) is combined with external to the core. The value of this bus is visible to software in the <i>IntCtl<sub>IPPCI</sub></i> register field.
<i>SI_IPTI[2:0]</i>	S	Indicates the <i>SI_Int</i> hardware interrupt pin that the timer interrupt pin ( <i>SI_TimerInt</i> ) is combined with external to the core. The value of this bus is visible to software in the <i>IntCtl<sub>IPTI</sub></i> register field.

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description						
SI_PCInt	O	<p>Performance Counter Interrupt. Asserted when bit 31 of any of the performance counters is set. This hardware pin represents the state of the <i>Cause<sub>PC</sub></i> register field</p> <p>For Release 1 Interrupt Compatibility mode or Vectored Interrupt mode:</p> <p>In order for the core to take a performance counter interrupt, the <i>SI_PCInt</i> signal needs to be brought back into the core on one of the six <i>SI_Int</i> interrupt pins in a system-dependent manner. Traditionally, this has been accomplished by muxing <i>SI_PCInt</i> with <i>SI_Int[5]</i>. Exposing <i>SI_PCInt</i> as an output allows more flexibility for the system designer. Performance counter interrupts can be muxed or ORed into one of the interrupts, as desired in a particular system. The <i>SI_Int</i> hardware interrupt pin with which the <i>SI_PCInt</i> signal is merged is indicated via the <i>SI_IPPCI</i> static input pins.</p> <p>For External Interrupt Controller (EIC) mode:</p> <p>The <i>SI_PCInt</i> signal is provided to the external interrupt controller, which then prioritizes the performance counter interrupt with all other interrupt sources, as desired. The controller then encodes the desired interrupt value on the <i>SI_Int</i> pins. Since <i>SI_Int</i> is usually encoded, the <i>SI_IPPCI</i> pins are not meaningful in EIC mode.</p>						
SI_SWInt[1:0]	O	Software interrupt request. These signals represent the value in the <i>IP[1:0]</i> field of the <i>Cause</i> register. They are provided for use by an external interrupt controller.						
SI_TimerInt	O	<p>Timer interrupt indication. This signal is asserted whenever the <i>Count</i> and <i>Compare</i> registers match and is deasserted when the <i>Compare</i> register is written. This hardware pin represents the value of the <i>Cause<sub>TI</sub></i> register field.</p> <p>Like <i>SI_PCInt</i>, this signal should be brought back into the core via one of the <i>SI_Int</i> pins. For compatibility or vectored interrupt mode, <i>SI_IPTI</i> should indicate which interrupt pin it has been merged with.</p>						
<i>Configuration Inputs:</i>								
SI_SBlock	S	<p>Controls the ordering of double-words within a bursted read request on the OCP interface. The value of this pin is visible in the <i>BM</i> field of the <i>Config0</i> register.</p> <table border="1" data-bbox="717 1146 1252 1260"> <thead> <tr> <th><i>SI_SBlock</i></th> <th>Burst Order</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Sequential</td> </tr> <tr> <td>1</td> <td>Subblock</td> </tr> </tbody> </table>	<i>SI_SBlock</i>	Burst Order	0	Sequential	1	Subblock
<i>SI_SBlock</i>	Burst Order							
0	Sequential							
1	Subblock							
SI_CPUNum[9:0]	S	Unique identifier to specify an individual core in a multi-processor system. The hardware value specified on these pins is available in the <i>CPUNum</i> field of the <i>EBase</i> register, so it can be used by software to distinguish a particular processor. In a single processor system, this value should be set to zero.						
SI_Endian	S	<p>Indicates the base endianness of the core. The value of this pin is visible in the <i>BE</i> field of the <i>Config0</i> register.</p> <table border="1" data-bbox="721 1514 1255 1627"> <thead> <tr> <th><i>EB_Endian</i></th> <th>Base Endian Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Little Endian</td> </tr> <tr> <td>1</td> <td>Big Endian</td> </tr> </tbody> </table>	<i>EB_Endian</i>	Base Endian Mode	0	Little Endian	1	Big Endian
<i>EB_Endian</i>	Base Endian Mode							
0	Little Endian							
1	Big Endian							

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																				
<i>SI_SimpleBE</i>	S	<p>The state of this signal can constrain the core to only generate certain byte enables on external interface transactions. This eases connection to some existing bus standards. The value of this pin is visible in the SB field of the <i>Config0</i> register.</p> <table border="1"> <thead> <tr> <th><i>SI_SimpleBE</i></th> <th>Byte Enable Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>All BEs allowed</td> </tr> <tr> <td>1</td> <td>Naturally aligned bytes, halfwords, words, and doublewords only</td> </tr> </tbody> </table>	<i>SI_SimpleBE</i>	Byte Enable Mode	0	All BEs allowed	1	Naturally aligned bytes, halfwords, words, and doublewords only														
<i>SI_SimpleBE</i>	Byte Enable Mode																					
0	All BEs allowed																					
1	Naturally aligned bytes, halfwords, words, and doublewords only																					
<i>SI_DMA_Priority</i>	I	Force the DMA to have a higher priority																				
<i>SI_IDMA_Priority</i>	I	DMA request should be higher priority than core requests																				
<i>SI_Ibs[3:0]</i>	O	This signal reflects the state of the BS bits[3:0] in the Instruction Breakpoint Status (IBS) register when EJTAG hardware breakpoint for instruction is implemented.																				
<i>SI_Dbs[1:0]</i>	O	This signal reflects the state of the BS bits[1:0] in the Data Breakpoint Status (IBS) register when EJTAG hardware breakpoint for data is implemented.																				
<p><b>L2 Interface:</b> Static inputs are needed to set up the CP0 <i>Config2</i> register if a Level 2 cache is present. Additional inputs are provided for performance counters related to an L2 cache.</p>																						
<i>L2_LineSize[3:0]</i>	S	<p>Encoded line size of the external L2 cache. The value of these pins is visible in the SL field of the <i>Config2</i> register. Note that a value of 0 indicates that no L2 cache is present.</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>L2 Line Size (bytes)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No L2 cache present</td> </tr> <tr> <td>1</td> <td>4</td> </tr> <tr> <td>2</td> <td>8</td> </tr> <tr> <td>3</td> <td>16</td> </tr> <tr> <td>4</td> <td>32</td> </tr> <tr> <td>5</td> <td>64</td> </tr> <tr> <td>6</td> <td>128</td> </tr> <tr> <td>7</td> <td>256</td> </tr> <tr> <td>8-15</td> <td>Reserved</td> </tr> </tbody> </table>	Encoding	L2 Line Size (bytes)	0	No L2 cache present	1	4	2	8	3	16	4	32	5	64	6	128	7	256	8-15	Reserved
Encoding	L2 Line Size (bytes)																					
0	No L2 cache present																					
1	4																					
2	8																					
3	16																					
4	32																					
5	64																					
6	128																					
7	256																					
8-15	Reserved																					

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																				
<i>L2_Sets[3:0]</i>	S	<p>Encoded number of L2 sets per way. The value of these pins is visible in the SS field of the <i>Config2</i> register.</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>L2 Sets Per Way</th> </tr> </thead> <tbody> <tr><td>0</td><td>64</td></tr> <tr><td>1</td><td>128</td></tr> <tr><td>2</td><td>256</td></tr> <tr><td>3</td><td>512</td></tr> <tr><td>4</td><td>1024</td></tr> <tr><td>5</td><td>2048</td></tr> <tr><td>6</td><td>4096</td></tr> <tr><td>7</td><td>8192</td></tr> <tr><td>8-15</td><td>Reserved</td></tr> </tbody> </table>	Encoding	L2 Sets Per Way	0	64	1	128	2	256	3	512	4	1024	5	2048	6	4096	7	8192	8-15	Reserved
Encoding	L2 Sets Per Way																					
0	64																					
1	128																					
2	256																					
3	512																					
4	1024																					
5	2048																					
6	4096																					
7	8192																					
8-15	Reserved																					
<i>L2_Assoc[3:0]</i>	S	<p>Encoded associativity of the L2 cache. The value of these pins is visible in the SA field of the <i>Config2</i> register.</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>L2 Associativity</th> </tr> </thead> <tbody> <tr><td>0</td><td>Direct mapped</td></tr> <tr><td>1</td><td>2</td></tr> <tr><td>2</td><td>3</td></tr> <tr><td>3</td><td>4</td></tr> <tr><td>4</td><td>5</td></tr> <tr><td>5</td><td>6</td></tr> <tr><td>6</td><td>7</td></tr> <tr><td>7</td><td>8</td></tr> <tr><td>8-15</td><td>Reserved</td></tr> </tbody> </table>	Encoding	L2 Associativity	0	Direct mapped	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8-15	Reserved
Encoding	L2 Associativity																					
0	Direct mapped																					
1	2																					
2	3																					
3	4																					
4	5																					
5	6																					
6	7																					
7	8																					
8-15	Reserved																					
<i>L2_PCWB</i>	I	Performance counter input. Indicates the number of L2 write backs (WB). One pulse (OCP clock width) per L2 WB event. The count is visible in CP0 <i>Performance Counter Register 0 Count</i> .																				
<i>L2_PCAcc</i>	I	Performance counter input. Indicates the number of L2 accesses. One pulse (OCP clock width) per L2 access event. The count is visible in CP0 <i>Performance Counter Register 1 Count</i> .																				
<i>L2_PCMiss</i>	I	Performance counter input. Indicates the number of L2 misses. One pulse (OCP clock width) per L2 miss event. The count is visible in CP0 <i>Performance Counter Register 0 and 1 Count</i> .																				
<i>L2_PCMissCy</i>	I	<p>Performance counter input. Indicates the number of cycles the L2 is held due to misses. Note that this is not an <i>event</i> unlike <i>L2_PCWB</i>, <i>L2_PCAcc</i>, or <i>L2_PCMiss</i>. 1 pulse (OCP clock width) per L2 miss cycle. Also note that the count is in terms of OCP cycles and not <i>SI_ClkIn</i> clock cycles. This needs to be factored in while reading this counter.</p> <p>Note: the count related to this signal is not currently visible in a CP0 <i>Performance Counter Register</i>.</p> <p>These 4 inputs can be redefined if no L2 is present or if desired. The count will in this case contain the number of OCP clock cycles this signal was high.</p>																				
<b>OCP Master System Interface:</b> These signals connect to the OCP Standard Master Interface.																						

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																				
<i>OC_MCmd[2:0]</i>	O	<p>OCP command bus, indicates the type of transaction requested. Only some encoding are used and they are set in concert with the values on OC_MReqInfo and OC_MAddrSpace. The encoding used by the 24Kc core are shown in the following table:</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>Command</th> <th>Mnemonic</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Idle</td> <td>IDLE</td> <td>No transaction</td> </tr> <tr> <td>1</td> <td>Write</td> <td>WR</td> <td>Used for data write and L2 CACHE write or invalidate</td> </tr> <tr> <td>2</td> <td>Read</td> <td>RD</td> <td>Used for fetch or data read or L2 CACHE reads or SYNC.</td> </tr> <tr> <td>3-7</td> <td>Unused</td> <td>-</td> <td>Not used on 24Kc core</td> </tr> </tbody> </table>	Encoding	Command	Mnemonic	Description	0	Idle	IDLE	No transaction	1	Write	WR	Used for data write and L2 CACHE write or invalidate	2	Read	RD	Used for fetch or data read or L2 CACHE reads or SYNC.	3-7	Unused	-	Not used on 24Kc core
		Encoding	Command	Mnemonic	Description																	
		0	Idle	IDLE	No transaction																	
		1	Write	WR	Used for data write and L2 CACHE write or invalidate																	
		2	Read	RD	Used for fetch or data read or L2 CACHE reads or SYNC.																	
3-7	Unused	-	Not used on 24Kc core																			

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																																						
<i>OC_MReqInfo</i> [3:0]	O	<p>OCP command bus extension.</p> <p><i>For transactions other than SYNC and CACHE, the OC_MReqInfo</i>[2:0] field encodes the cacheability attributes for a transaction; it uses the same encoding as the CCA field described in Table 7 on page 14.</p> <p><i>OC_MReqInfo</i>[3] indicates that the transaction is due to a SYNC instruction; when this bit is high, the lower bits [2:0] indicate an uncached CCA type.</p> <p>The encoding of the <i>OC_MReqInfo</i> field for all transactions other than CACHE is summarized in the following sub-table:</p> <p style="text-align: center;"><b>Encoding for all transactions other than CACHE</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Encoding</th> <th>Command Information</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>cacheable, noncoherent, WT, NWA</td> </tr> <tr> <td>1</td> <td>reserved</td> </tr> <tr> <td>2</td> <td>uncached</td> </tr> <tr> <td>3</td> <td>cacheable, noncoherent, WB, WA</td> </tr> <tr> <td>4-6</td> <td>reserved</td> </tr> <tr> <td>7</td> <td>uncached accelerated</td> </tr> <tr> <td>8-9</td> <td>reserved</td> </tr> <tr> <td>10</td> <td>SYNC with uncached CCA</td> </tr> <tr> <td>11-15</td> <td>reserved</td> </tr> </tbody> </table> <p>If the transaction is a CACHE transaction to an off-core L2/L3 cache, then the lower 3 bits of <i>OC_MReqInfo</i> are identical to bits 20:18 of the CACHE opcode and indicate the type of operation (See the <i>MIPS32 24K Processor Core Family Software User's Manual</i> for details). This encoding is shown in the sub-table below. Note that a L2/L3 CACHE transaction is identified when one of the bits of <i>MAddrSpace</i>[1:0] are set to 1.</p> <p>The encoding of the <i>OC_MReqInfo</i> field for the CACHE transaction is summarized in the following sub-table:</p> <p style="text-align: center;"><b>Encoding for CACHE transaction</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Encoding</th> <th>Command Information</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>index Writeback Invalidate/ Index Invalidate</td> </tr> <tr> <td>1</td> <td>index Load Tag</td> </tr> <tr> <td>2</td> <td>index Store Tag</td> </tr> <tr> <td>3</td> <td>reserved</td> </tr> <tr> <td>4</td> <td>hit invalidate</td> </tr> <tr> <td>5</td> <td>hit writeback invalidate/ hit invalidate</td> </tr> <tr> <td>6</td> <td>hit writeback</td> </tr> <tr> <td>7-15</td> <td>reserved</td> </tr> </tbody> </table>	Encoding	Command Information	0	cacheable, noncoherent, WT, NWA	1	reserved	2	uncached	3	cacheable, noncoherent, WB, WA	4-6	reserved	7	uncached accelerated	8-9	reserved	10	SYNC with uncached CCA	11-15	reserved	Encoding	Command Information	0	index Writeback Invalidate/ Index Invalidate	1	index Load Tag	2	index Store Tag	3	reserved	4	hit invalidate	5	hit writeback invalidate/ hit invalidate	6	hit writeback	7-15	reserved
Encoding	Command Information																																							
0	cacheable, noncoherent, WT, NWA																																							
1	reserved																																							
2	uncached																																							
3	cacheable, noncoherent, WB, WA																																							
4-6	reserved																																							
7	uncached accelerated																																							
8-9	reserved																																							
10	SYNC with uncached CCA																																							
11-15	reserved																																							
Encoding	Command Information																																							
0	index Writeback Invalidate/ Index Invalidate																																							
1	index Load Tag																																							
2	index Store Tag																																							
3	reserved																																							
4	hit invalidate																																							
5	hit writeback invalidate/ hit invalidate																																							
6	hit writeback																																							
7-15	reserved																																							

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																		
<i>OC_MAddrSpace[1:0]</i>	O	<p>L2/L3 Address Space indicator. When the 24Kc core is issuing an L2 or an L3 CACHE operation, the corresponding bit (Bit [0] for L2, and Bit [1] for L3) is asserted. It indicates to the system that this OCP command is targeted to the address space of the L2 or L3 Cache.</p> <p>The encoding of this field is summarized in the following table:</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>Address Space</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal address space</td> </tr> <tr> <td>1</td> <td>L2 address space</td> </tr> <tr> <td>2</td> <td>L3 address space</td> </tr> <tr> <td>3</td> <td>reserved</td> </tr> </tbody> </table>	Encoding	Address Space	0	Normal address space	1	L2 address space	2	L3 address space	3	reserved								
Encoding	Address Space																			
0	Normal address space																			
1	L2 address space																			
2	L3 address space																			
3	reserved																			
<i>OC_MAddr[31:3]</i>	O	<p>Physical doubleword address bus. Note that the least significant 3 address bits not included in this bus are decoded in the read (<i>OC_MByteEn</i>) or write (<i>OC_MDataByteEn</i>) byte enable fields. When <i>OC_MAddrSpace[1:0]</i> is not zero (to indicate a CACHE operation), then <i>OC_MAddr[31:5]</i> carries the cache line address (or the cache line index for Indexed CACHE ops).</p>																		
<i>OC_MBurstSeq[2:0]</i>	O	<p>Indicates type of burst sequence. The 24Kc core can only generate two possible values, determined by the <i>SI_SBlock</i> static input, as shown in the following table:</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>Burst Sequence</th> </tr> </thead> <tbody> <tr> <td>2</td> <td>Sequential: Critical dword first, with linear wrapping for subsequent beats.</td> </tr> <tr> <td>4</td> <td>Sub-block: Critical dword first, with increment/decrement for subsequent beats</td> </tr> <tr> <td>0-1,3,5-7</td> <td>Unused by 24Kc core</td> </tr> </tbody> </table>	Encoding	Burst Sequence	2	Sequential: Critical dword first, with linear wrapping for subsequent beats.	4	Sub-block: Critical dword first, with increment/decrement for subsequent beats	0-1,3,5-7	Unused by 24Kc core										
Encoding	Burst Sequence																			
2	Sequential: Critical dword first, with linear wrapping for subsequent beats.																			
4	Sub-block: Critical dword first, with increment/decrement for subsequent beats																			
0-1,3,5-7	Unused by 24Kc core																			
<i>OC_MTagID[2:0]</i>	O	<p>Transaction tag identifier. The encoding of this field is determined by the BIU buffer holding the outstanding transaction, as shown in the following table. Note: the 24Kc core assumes a non-reordering subset of the OCP Tag semantics. For more explanation, see "<a href="#">OCP Interface Transactions</a>" on page 54.</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>Tag Allocation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>From Read buffer 0</td> </tr> <tr> <td>1</td> <td>From Read buffer 1</td> </tr> <tr> <td>2</td> <td>From Read buffer 2</td> </tr> <tr> <td>3</td> <td>From Read buffer 3</td> </tr> <tr> <td>4</td> <td>From Fetch buffer 0</td> </tr> <tr> <td>5</td> <td>From Fetch buffer 1</td> </tr> <tr> <td>6</td> <td>SYNC</td> </tr> <tr> <td>7</td> <td>WR, CACHE-RD, CACHE-WR</td> </tr> </tbody> </table>	Encoding	Tag Allocation	0	From Read buffer 0	1	From Read buffer 1	2	From Read buffer 2	3	From Read buffer 3	4	From Fetch buffer 0	5	From Fetch buffer 1	6	SYNC	7	WR, CACHE-RD, CACHE-WR
Encoding	Tag Allocation																			
0	From Read buffer 0																			
1	From Read buffer 1																			
2	From Read buffer 2																			
3	From Read buffer 3																			
4	From Fetch buffer 0																			
5	From Fetch buffer 1																			
6	SYNC																			
7	WR, CACHE-RD, CACHE-WR																			
<i>OC_MBurstPrecise</i>	SO	<p>Indicates whether the burst length is precise. In the 24Kc core, burst lengths are always fixed at 4 beats, so this pin is statically set to 0x1.</p>																		
<i>OC_MBurstSingleReq</i>	SO	<p>Indicates whether there is a single request for all data transfers in a burst. In the 24Kc core, there is always a single command request so this pin is statically set to 0x1.</p>																		



Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																		
<i>OC_MBurstLength[2:0]</i>	O	<p>Number of 64b data transfers. Only two values are possible in the 24Kc core.</p> <table border="1"> <thead> <tr> <th>Encoding</th> <th>Number of Transfers</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1, single transfer</td> </tr> <tr> <td>4</td> <td>4-beat burst</td> </tr> <tr> <td>others</td> <td>Unused by 24Kc core</td> </tr> </tbody> </table>	Encoding	Number of Transfers	1	1, single transfer	4	4-beat burst	others	Unused by 24Kc core										
Encoding	Number of Transfers																			
1	1, single transfer																			
4	4-beat burst																			
others	Unused by 24Kc core																			
<i>OC_MByteEn[7:0]</i>	O	<p>Byte enables for reads. Includes data alignment, endianness and address. The correlation of each bit in the <i>OC_MByteEn</i> field to the returned read data bytes is shown in the following table:</p> <table border="1"> <thead> <tr> <th><i>OC_MByteEn</i> signal</th> <th>Requested byte to be returned on <i>OC_SData</i> bus</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>[7:0]</td> </tr> <tr> <td>[1]</td> <td>[15:8]</td> </tr> <tr> <td>[2]</td> <td>[23:16]</td> </tr> <tr> <td>[3]</td> <td>[31:24]</td> </tr> <tr> <td>[4]</td> <td>[39:32]</td> </tr> <tr> <td>[5]</td> <td>[47:40]</td> </tr> <tr> <td>[6]</td> <td>[55:48]</td> </tr> <tr> <td>[7]</td> <td>[63:56]</td> </tr> </tbody> </table>	<i>OC_MByteEn</i> signal	Requested byte to be returned on <i>OC_SData</i> bus	[0]	[7:0]	[1]	[15:8]	[2]	[23:16]	[3]	[31:24]	[4]	[39:32]	[5]	[47:40]	[6]	[55:48]	[7]	[63:56]
<i>OC_MByteEn</i> signal	Requested byte to be returned on <i>OC_SData</i> bus																			
[0]	[7:0]																			
[1]	[15:8]																			
[2]	[23:16]																			
[3]	[31:24]																			
[4]	[39:32]																			
[5]	[47:40]																			
[6]	[55:48]																			
[7]	[63:56]																			
<i>OC_MData[63:0]</i>	O	Write data bus from the 24Kc core.																		
<i>OC_MDataByteEn[7:0]</i>	O	<p>Byte enables for writes. Includes data alignment, endianness and address. The correlation of each bit in the <i>OC_MDataByteEn</i> field to the write data bytes is shown in the following table. Note that the 24Kc core does not use <i>OC_MByteEn</i> for transferring byte enables during writes as some other OCP masters do.</p> <table border="1"> <thead> <tr> <th><i>OC_MDataByteEn</i> signal</th> <th>Valid write data byte on <i>OC_MData</i> bus</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>[7:0]</td> </tr> <tr> <td>[1]</td> <td>[15:8]</td> </tr> <tr> <td>[2]</td> <td>[23:16]</td> </tr> <tr> <td>[3]</td> <td>[31:24]</td> </tr> <tr> <td>[4]</td> <td>[39:32]</td> </tr> <tr> <td>[5]</td> <td>[47:40]</td> </tr> <tr> <td>[6]</td> <td>[55:48]</td> </tr> <tr> <td>[7]</td> <td>[63:56]</td> </tr> </tbody> </table>	<i>OC_MDataByteEn</i> signal	Valid write data byte on <i>OC_MData</i> bus	[0]	[7:0]	[1]	[15:8]	[2]	[23:16]	[3]	[31:24]	[4]	[39:32]	[5]	[47:40]	[6]	[55:48]	[7]	[63:56]
<i>OC_MDataByteEn</i> signal	Valid write data byte on <i>OC_MData</i> bus																			
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[4]	[39:32]																			
[5]	[47:40]																			
[6]	[55:48]																			
[7]	[63:56]																			
<i>OC_MDataValid</i>	O	Valid write data on <i>OC_MData</i> bus.																		
<i>OC_MDataTagID[2:0]</i>	O	Write data tag identifier (for out of order returns). Per the encoding for <i>OC_MTagID</i> , the only valid value in the 24Kc core is 0x7.																		
<i>OC_MDataLast</i>	O	Last valid data in a write burst.																		
<i>OC_SData[63:0]</i>	I	Returned read data to core.																		
<i>OC_STagID[2:0]</i>	I	Return transaction tag ID. See <i>OC_MTagID</i> for encoding.																		

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																				
<i>OC_SResp[1:0]</i>	I	Valid response from system controller. The encoding recognized by the 24Kc core are shown in the following table																				
		<table border="1"> <thead> <tr> <th>Encoding</th> <th>Command</th> <th>Mnemonic</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No response</td> <td>NULL</td> <td>No response</td> </tr> <tr> <td>1</td> <td>Data valid / accept</td> <td>DVA</td> <td>Normal completion response</td> </tr> <tr> <td>2</td> <td>Reserved</td> <td>-</td> <td>Should not be used on 24Kc core</td> </tr> <tr> <td>3</td> <td>Response error</td> <td>ERR</td> <td>Signals bus error exception</td> </tr> </tbody> </table>	Encoding	Command	Mnemonic	Description	0	No response	NULL	No response	1	Data valid / accept	DVA	Normal completion response	2	Reserved	-	Should not be used on 24Kc core	3	Response error	ERR	Signals bus error exception
		Encoding	Command	Mnemonic	Description																	
		0	No response	NULL	No response																	
		1	Data valid / accept	DVA	Normal completion response																	
2	Reserved	-	Should not be used on 24Kc core																			
3	Response error	ERR	Signals bus error exception																			
<i>OC_SRespLast</i>	I	Marks last data in read burst.																				
<i>OC_SCmdAccept</i>	I	System controller notifies the 24Kc core that the command is accepted.																				
<i>OC_SDataAccept</i>	I	System Controller notifies the 24Kc core that the write data is accepted.																				
<i>OC_MTagInOrder</i>	SO	Indicates if the request can be reordered. This pin is statically tied to 0x0.																				
<p><b>CorExtend/MDU Interface:</b> On 24Kc Pro cores, there is an external interface to a combined CorExtend and MDU block. Refer to the <i>MIPS32™ 24K™ Pro Series™ CorExtend™ Instruction Integrator's Guide</i> for more details on these signals.</p>																						
<p><b>Coprocessor 2 Interface</b></p>																						
<i>CP2_gfclk</i>	O	Free running clock for coprocessor 2. Same as <i>SI_ClkIn</i>																				
<i>CP2_gclk</i>	O	Gated coprocessor 2 clock																				
<i>CP2_gscanenable</i>	O	Scanenable for coprocessor 2 module. This is same as <i>gscanenable</i> .																				
<p><b>Dispatch:</b> These signals are used to transfer an instruction from the 24Kc core to the COP2 coprocessor.</p>																						
<i>CP2_ir_0[31:0]</i>	O	Coprocessor Instruction Word. <i>Valid in the cycle before CP2_as_0, CP2_ts_0 or CP2_fs_0.</i>																				
<i>CP2_irenable_0</i>	O	Enable Instruction Registering. <i>When deasserted, no instruction strobes will be asserted in the following cycle.</i>																				
<i>CP2_as_0</i>	O	Coprocessor 2 Arithmetic Instruction Strobe.																				
<i>CP2_abusy_0</i>	I	Coprocessor 2 Arithmetic Busy.																				
<i>CP2_ts_0</i>	O	Coprocessor 2 To Strobe.																				
<i>CP2_tbusy_0</i>	I	To Coprocessor 2 Busy.																				
<i>CP2_fs_0</i>	O	Coprocessor 2 From Strobe.																				
<i>CP2_fbusy_0</i>	I	From Coprocessor 2 Busy.																				
<i>CP2_endian_0</i>	O	Big Endian Byte Ordering. <i>Valid the cycle before CP2_as_0, CP2_fs_0 or CP2_ts_0.</i>																				
<i>CP2_inst32_0</i>	SO	MIPS32 Compatibility Mode - Instructions. <i>Valid the cycle before CP2_as_0, CP2_fs_0 or CP2_ts_0.</i> <b>Tied high in 24K.</b>																				
<i>CP2_kd_mode_0</i>	O	Kernel/Debug mode. When asserted, the processor is in kernel or debug mode. <i>Valid the cycle before CP2_as_0, CP2_fs_0 or CP2_ts_0 is asserted.</i>																				
<p><b>To COP Data transfer:</b> These signals are used when data is sent from the 24Kc core to the COP2 coprocessor, as part of completing a To Coprocessor instruction.</p>																						

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description
<i>CP2_tds_0</i>	O	Coprocessor To Data Strobe.
<i>CP2_torder_0[2:0]</i>	SO	Coprocessor To Order. No out-of-order data to COP2. <b>Forced to 000.</b>
<i>CP2_tordlim_0[2:0]</i>	I	To Coprocessor Data Out-of-order Limit. <b>Being ignored.</b>
<i>CP2_tdata_0[63:0]</i>	O	To Coprocessor Data.
<b>From COP Data transfer:</b> These signals are used when data is sent to the 24Kc core from the COP2 coprocessor, as part of completing a From Coprocessor instruction.		
<i>CP2_fds_0</i>	I	Coprocessor From Data Strobe.
<i>CP2_forder_0[2:0]</i>	I	Coprocessor From Order. No out-of-order support in 24K. <b>Expected to be 000 in 24K.</b>
<i>CP2_fordlim_0[2:0]</i>	SO	From Coprocessor Data Out-of-order Limit. No out-of-order data to COP2. <b>Forced to 000 in 24K.</b>
<i>CP2_fdata_0[63:0]</i>	I	From Coprocessor Data.
<b>COP Condition Code Check:</b> These signals are used to report the result of a condition code check to the 24Kc core from the COP2 coprocessor. This is only used for BC2 instructions.		
<i>CP2_cccs_0</i>	I	Coprocessor Condition Code Check Strobe.
<i>CP2_ccc_0</i>	I	Coprocessor Condition Code Check. <i>When asserted, the branch should take the branch.</i> <i>When deasserted, the branch should not take the branch.</i>
<b>Exceptions:</b> These signals are used by the COP2 coprocessor to report exception for each instruction.		
<i>CP2_excxs_0</i>	I	Coprocessor Exception Strobe.
<i>CP2_exc_0</i>	I	Coprocessor Exception. Valid when CP2_excxs_0 is asserted.
<i>CP2_exccode_0[4:0]</i>	I	Coprocessor Exception Code. Valid when both CP2_excxs_0 and CP2_exc_0 are asserted. <ul style="list-style-type: none"> <li>• 01010: RI (This will trigger RI in core pipeline.)</li> <li>• 10000: Available for Coprocessor specific exception</li> <li>• 10010: C2E exception.</li> <li>• All others: Reserved</li> </ul>
<b>Nullification:</b> These signals are used by the 24Kc core to signal nullification of each instruction to the COP2 coprocessor.		
<i>CP2_nulls_0</i>	O	Coprocessor Null Strobe.
<i>CP2_null_0</i>	O	Nullify coprocessor instruction.
<b>Kill:</b> These signals are used by the 24Kc core to signal killing of each instruction to the COP2 coprocessor.		
<i>CP2_kills_0</i>	O	Coprocessor Kill Strobe.

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description
<i>CP2_kill_0[1:0]</i>	O	Kill Coprocessor Instruction. <ul style="list-style-type: none"> <li>• 00 / 01: Instruction is not killed. OK for commit.</li> <li>• 10: Instruction is killed not due to CP2_exc.</li> <li>• 11: Instruction is killed due to CP2_exc.</li> </ul>
<b>Miscellaneous COP2 signals:</b>		
<i>CP2_reset</i>	O	Coprocessor Reset. Asserted when a reset is performed by the integer pipeline.
<i>CP2_present</i>	S	COP2 Present.
<i>CP2_idle</i>	I	Coprocessor Idle. Asserted when the coprocessor logic is idle. <i>Enables the processor to go into sleep mode and shut down the clock.</i>
<i>CP2_perfcnt_event</i>	I	Implementation coprocessor performance counter event.
<i>CP2_tx32</i>	S	COP2 32-bit Transfers. When this signal is asserted, the integer unit must cause an RI exception for 64-bit COP2 TF instructions.
<b>Data scratchpad RAM (DSPRAM) Interface:</b>		
This set of interface signals allows the data scratchpad RAM array to be accessed independent of the data cache.		
Note: In order to achieve single cycle access, the ScratchPad interface is not fully registered, unlike most other core interfaces. This requires more careful timing considerations.		
<i>SP_gfclk</i>	O	DSPRAM free running clock. This signal follow <i>SI_ClkIn</i>
<i>SP_gclk</i>	O	DSPRAM gated clock. This clock is shutdown when the processor is in sleep mode and top level clock gating is enabled.
<i>SP_greset_pre</i>	O	This reset signal should be registered within the DSPRAM module before use. The registered version of this signal follows the reset seen by rest of the core logic.
<i>SP_gscanenable</i>	O	Scanenable signal for DSPRAM module. This signal follows the gscanenable to the core.
<i>SP_parity_en</i>	O	DSPRAM parity enable
<i>SP_sleep_req_xx</i>	O	Asserted when entering sleep mode, the clock will be killed in the next cycle
<i>SP_wait_pd_xx</i>	O	A WAIT instruction pending in the pipeline
<i>SP_tag_rd_ag</i>	O	DSPRAM Tag Read Strobe. Asserted when a read on DSPRAM tag register (either base address or size register) is performed
<i>SP_tag_wr_ag</i>	O	DSPRAM Tag Write Strobe. Asserted when a write to DSPRAM tag register (either base address or size register) is performed
<i>SP_tag_sel_ag</i>	O	DSPRAM Tag read/write selection (0: base address register, 1: size register)
<i>SP_tag_wdata_ag[31:11]</i>	O	DSPRAM Tag write data. It is valid when <i>SP_tag_wr_ag</i> is asserted
<i>SP_data_addr_ag[19:2]</i>	O	Address of the SPRAM data access. This is valid during the cycle that <i>SP_data_rd_ag</i> or <i>SP_data_wr_ag</i> is asserted.
<i>SP_data_rd_ag</i>	O	DSPRAM data read strobe.
<i>SP_dma_rd_ag</i>	O	Indication that the read to DSPRAM is from a DMA request.
<i>SP_data_wr_ag</i>	O	DSPRAM data write strobe
<i>SP_data_wren_ag[7:0]</i>	O	DSPRAM Data Write mask. This is the byte enable for the write data to SPRAM. Only valid when <i>SP_data_wr_ag</i> is asserted

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																				
<i>SP_data_wdata_ag[63:0]</i>	O	DSPRAM write data.																				
<i>SP_data_wpar_ag[7:0]</i>	O	Byte parity bits for write data bus ( <i>SP_data_wdata_ag</i> )																				
<i>SP_req_id_ag[2:0]</i>	O	Request identification from the core to the SPRAM. This is used to track loads from DSPRAM. It is valid the cycle <i>SP_data_rd_ag</i> is asserted																				
<i>SP_core_reqpd_er</i>	O	Asserted when a SPRAM instruction is pending. No DMA access will be issued to DSPRAM. This signal will be ignored when <i>SI_DMA_Priority</i> = 1																				
<i>SP_mbsp_tosp_xx[n-1:0]</i>	O	User defined variable width DSPRAM BIST sideband signal to DSPRAM.																				
<i>SP_sp_tombasp_xx[n-1:0]</i>	I	User defined variable width DSPRAM BIST sideband signal from DSPRAM.																				
<i>SP_present</i>	S	Presence of SPRAM																				
<i>SP_parity_present</i>	I	Indicates if parity logic is implemented in the DSPRAM module																				
<i>SP_perfcnt_event</i>	I	Implementation specific SPRAM performance counter event																				
<i>SP_ram_busy</i>	I	This is used for a non-pipelined multi-cycle SPRAM design. Asserted when the SPRAM will not be able to take any request in the next cycle. Any access to SPRAM will be stalled in the next cycle.																				
<i>SP_busy_xx</i>	I	Asserted when SPRAM is not idle. This will prevent the processor from entering the sleep mode and disable the clock																				
<i>SP_tag_rdata_xx[31:11]</i>	I	DSPRAM tag read data																				
<i>SP_tag_msk_xx[31:12]</i>	I	Address mask for different size SPRAM Tag comparison. When the mask bit is one, the address bit will participate in the tag comparison. When the mask is zero, the address bit will be excluded from tag comparison																				
		<table border="1"> <thead> <tr> <th>SPRAM size</th> <th><i>SP_tag_msk_xx[31:12]</i></th> </tr> </thead> <tbody> <tr> <td>4KB</td> <td>1111_1111_1111_1111_1111</td> </tr> <tr> <td>8KB</td> <td>1111_1111_1111_1111_1110</td> </tr> <tr> <td>16KB</td> <td>1111_1111_1111_1111_1100</td> </tr> <tr> <td>32KB</td> <td>1111_1111_1111_1111_1000</td> </tr> <tr> <td>64KB</td> <td>1111_1111_1111_1111_0000</td> </tr> <tr> <td>128KB</td> <td>1111_1111_1111_1110_0000</td> </tr> <tr> <td>256KB</td> <td>1111_1111_1111_1100_0000</td> </tr> <tr> <td>512KB</td> <td>1111_1111_1111_1000_0000</td> </tr> <tr> <td>1MB</td> <td>1111_1111_1111_0000_0000</td> </tr> </tbody> </table>	SPRAM size	<i>SP_tag_msk_xx[31:12]</i>	4KB	1111_1111_1111_1111_1111	8KB	1111_1111_1111_1111_1110	16KB	1111_1111_1111_1111_1100	32KB	1111_1111_1111_1111_1000	64KB	1111_1111_1111_1111_0000	128KB	1111_1111_1111_1110_0000	256KB	1111_1111_1111_1100_0000	512KB	1111_1111_1111_1000_0000	1MB	1111_1111_1111_0000_0000
		SPRAM size	<i>SP_tag_msk_xx[31:12]</i>																			
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		16KB	1111_1111_1111_1111_1100																			
		32KB	1111_1111_1111_1111_1000																			
		64KB	1111_1111_1111_1111_0000																			
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		256KB	1111_1111_1111_1100_0000																			
512KB	1111_1111_1111_1000_0000																					
1MB	1111_1111_1111_0000_0000																					
<i>SP_data_rdata_xx[63:0]</i>	I	Data return form SPRAM read. It is valid the same cycle <i>SP_datavld_xx</i> is asserted. For single cycle access, read data should be returned the cycle after <i>SP_data_rd_ag</i> is asserted.																				
<i>SP_data_rpar_xx[7:0]</i>	I	Byte parity of SPRAM read data ( <i>SP_data_rdata_xx</i> ). It is valid the same cycle <i>SP_datavld_xx</i> is asserted. For a SPRAM design where no parity is implemented, this signal is ignored.																				
<i>SP_datavld_nxt_xx</i>	I	Indicates that is a valid return data from SPRAM for a read.																				
<i>SP_data_id_xx[2:0]</i>	I	Instruction identification associated with the data returned. This is valid the same cycle <i>SP_datavld_xx</i> is asserted.																				
<i>SP_dma_id_xx[2:0]</i>	I	OCP TagID of a DSPRAM DMA access. It is valid the same cycle <i>SP_dma_wr_ag</i> or <i>SP_dma_rd_ag</i> is asserted.																				

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																				
<i>SP_dma_addr_xx[19:3]</i>	I	Index of a DSPRAM DMA request. It is valid the same cycle <i>SP_dma_rd_ag</i> or <i>SP_dma_wr_ag</i> is asserted.																				
<i>SP_dma_wdata_xx[63:0]</i>	I	Write data for a DMA write request. It is valid the same cycle <i>SP_dma_wr_ag</i> is asserted.																				
<i>SP_dma_wren_xx[7:0]</i>	I	Byte write enable for a DMA write request.																				
<i>SP_dma_rd_xx</i>	I	DSPRAM DMA read strobe																				
<i>SP_dma_wr_xx</i>	I	DSPRAM DMA write strobe																				
<i>SP_dma_stallreq_xx</i>	I	Stall request from scratch pad to processor when there is a DMA access and <i>SI_DMA_Priority</i> = 1																				
<b>DSPRAM External Interface (OCP Slave Interface)</b> This set of interface signals allows a DMA device to access the optional data scratchpad RAM.																						
<i>OC_DMA_MCmd[2:0]</i>	I	OCP command bus indicating the type of transaction requested. The following are the encoding and the transaction type supported by the slave.																				
		<table border="1"> <thead> <tr> <th>Encoding</th> <th>Command</th> <th>Mnemonic</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Idle</td> <td>IDLE</td> <td>No transaction</td> </tr> <tr> <td>1</td> <td>Write</td> <td>WR</td> <td>Used for data write</td> </tr> <tr> <td>2</td> <td>Read</td> <td>RD</td> <td>Used for data read</td> </tr> <tr> <td>3-7</td> <td>Unused</td> <td>-</td> <td>Not used on 24Kc core</td> </tr> </tbody> </table>	Encoding	Command	Mnemonic	Description	0	Idle	IDLE	No transaction	1	Write	WR	Used for data write	2	Read	RD	Used for data read	3-7	Unused	-	Not used on 24Kc core
		Encoding	Command	Mnemonic	Description																	
		0	Idle	IDLE	No transaction																	
		1	Write	WR	Used for data write																	
2	Read	RD	Used for data read																			
3-7	Unused	-	Not used on 24Kc core																			
<i>OC_DMA_MTagID[2:0]</i>	I	Transaction tag identifier.																				
<i>OC_DMA_MAddr[31:3]</i>	I	Physical doubleword address bus. This address should fall in the address range programmed in the DSPRAM module.																				
<i>OC_DMA_MByteEn[7:0]</i>	I	Byte enable for reads operation. In combination with the endianness this bus determines the byte addressed for the read operation. The correlation of each bit in the <i>OC_DMA_MByteEn</i> field to the returned read data bytes is shown in the following table:																				
		<table border="1"> <thead> <tr> <th><i>OC_DMA_MByteEn</i> signal</th> <th>Requested byte to be returned on <i>OC_DMA_SData</i> bus</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>[7:0]</td> </tr> <tr> <td>[1]</td> <td>[15:8]</td> </tr> <tr> <td>[2]</td> <td>[23:16]</td> </tr> <tr> <td>[3]</td> <td>[31:24]</td> </tr> <tr> <td>[4]</td> <td>[39:32]</td> </tr> <tr> <td>[5]</td> <td>[47:40]</td> </tr> <tr> <td>[6]</td> <td>[55:48]</td> </tr> <tr> <td>[7]</td> <td>[63:56]</td> </tr> </tbody> </table>	<i>OC_DMA_MByteEn</i> signal	Requested byte to be returned on <i>OC_DMA_SData</i> bus	[0]	[7:0]	[1]	[15:8]	[2]	[23:16]	[3]	[31:24]	[4]	[39:32]	[5]	[47:40]	[6]	[55:48]	[7]	[63:56]		
		<i>OC_DMA_MByteEn</i> signal	Requested byte to be returned on <i>OC_DMA_SData</i> bus																			
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		[1]	[15:8]																			
		[2]	[23:16]																			
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		[4]	[39:32]																			
		[5]	[47:40]																			
[6]	[55:48]																					
[7]	[63:56]																					
<i>OC_DMA_MDataTagID[2:0]</i>	I	Write data tag identifier																				
<i>OC_DMA_MData[63:0]</i>	I	Write data bus to the data scratchpad RAM																				
<i>OC_DMA_MDataByteEn[7:0]</i>	I	Byte lane selection for write data																				
<i>OC_DMA_MDataValid</i>	I	Write data ( <i>OC_DMA_MData</i> ) valid indication																				

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description
<i>OC_DMA_SResp[1:0]</i>	O	Read/Write response (00=NULL, 01=VALID 11=ERR)
<i>OC_DMA_STagID[2:0]</i>	O	Return transaction tag ID.
<i>OC_DMA_SData[63:0]</i>	O	Return data read from the scratchpad RAM.
<i>OC_DMA_SCmdAccept</i>	O	Flow control for commands (0=BUSY, 1=READY) <ul style="list-style-type: none"> <li>The core deasserts this signal when it is not ready to accept a new command. The master has to hold the new command till it is accepted by the core.</li> <li>The core asserts this signal when it has accepted a new command</li> </ul>
<i>OC_DMA_SDataAccept</i>	O	Flow control for data (0=BUSY, 1=READY) <ul style="list-style-type: none"> <li>The core deasserts this signal when it is not ready to accept a the data driven in <i>OC_DMA_SData</i>. The master has to hold the data till it is accepted by the core.</li> <li>The core asserts this signal when it has accepted the data driven in <i>OC_DMA_SData</i></li> </ul>
<b>Instruction scratchpad RAM (ISPRAM) Interface:</b>		
This set of interface signals allows the instruction scratchpad RAM array to be accessed independent of the instruction cache.		
Note: In order to achieve single cycle access, the ScratchPad interface is not fully registered, unlike most other core interfaces. This requires more careful timing considerations		
<i>ISP_gclk</i>	O	Gated global clock
<i>ISP_gfclk</i>	O	Free-running global clock
<i>ISP_greset_pre</i>	O	Global reset. Must be registered prior to use
<i>ISP_gscanenable</i>	O	Global scanenable. Use to override local clock gating during scan.
<i>ISP_parity_en</i>	O	ISPRAM parity enable - used to control whether parity errors on DMA reads are reported or not.
<i>ISP_wait_pd_xx</i>	O	WAIT instruction has been executed and core is getting ready to go to sleep
<i>ISP_sleep_req_xx</i>	O	Entering sleep mode in the next cycle
<i>ISP_core_reqpd_xx</i>	O	There is a core access pending (stalling the DMA request)
<i>ISP_addr_ipf[19:3]</i>	O	Index for access.
<i>ISP_tag_sel_ipf</i>	O	Controls whether Size or base address register is written
<i>ISP_rd_ipf</i>	O	Read Strobe - both tag and data values are read
<i>ISP_dma_rd_ipf</i>	O	The read is a for a DMA access
<i>ISP_tag_wr_ipf</i>	O	Tag Write Strobe
<i>ISP_tag_wdata_ipf[31:11]</i>	O	Tag write data.
<i>ISP_data_wr_ipf</i>	O	Data Write Strobe
<i>ISP_data_wdata_ipf[69:0]</i>	O	Data write data (instructions + precode)
<i>ISP_data_wpar_ipf[8:0]</i>	O	Parity for write data
<i>ISP_present</i>	I	Presence of ISPRAM
<i>ISP_parity_present</i>	I	ISPRAM array has parity support

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																				
<i>ISP_perfcnt_event</i>	I	Implementation specific ISPRAM performance counter event																				
<i>ISP_ram_busy_</i>	I	ISPRAM will not accept any request in the next cycle																				
<i>ISP_busy_xx</i>	I	ISPRAM is busy with request - for sleep mode.																				
<i>ISP_tag_rdata_iff[31:11]</i>	I	Base address for SPRAM region.																				
<i>ISP_tag_msk_iff[19:12]</i>	I	Mask for address comparison																				
<i>ISP_data_rdata_is[69:0]</i>	I	Read data from data port																				
<i>ISP_data_rpar_is[8:0]</i>	I	Parity for read data																				
<i>ISP_datavld_next_if</i>	I	Read data will be valid next cycle																				
<i>ISP_dma_addr_xx[19:3]</i>	I	Index of DMA access																				
<i>ISP_dma_wdata_xx[63:0]</i>	I	DMA write data																				
<i>ISP_dma_rreq_xx</i>	I	DMA read request																				
<i>ISP_dma_wrreq_xx</i>	I	DMA write request																				
<i>ISP_dma_stallreq_xx</i>	I	DMA stall request to the core (when DMA has higher priority)																				
<b>ISPRAM External Interface (OCP Slave Interface)</b> This set of interface signals allows a DMA device to access the optional instruction scratchpad RAM.																						
<i>OC_IDMA_MCmd[2:0]</i>	I	<p>OCP command bus indicating the type of transaction requested. The following are the encoding and the transaction type supported by the slave.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Encoding</th> <th>Command</th> <th>Mnemonic</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Idle</td> <td>IDLE</td> <td>No transaction</td> </tr> <tr> <td>1</td> <td>Write</td> <td>WR</td> <td>Used for data write</td> </tr> <tr> <td>2</td> <td>Read</td> <td>RD</td> <td>Used for data read</td> </tr> <tr> <td>3-7</td> <td>Unused</td> <td>-</td> <td>Not used on 24Kc core</td> </tr> </tbody> </table>	Encoding	Command	Mnemonic	Description	0	Idle	IDLE	No transaction	1	Write	WR	Used for data write	2	Read	RD	Used for data read	3-7	Unused	-	Not used on 24Kc core
Encoding	Command	Mnemonic	Description																			
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3-7	Unused	-	Not used on 24Kc core																			
<i>OC_IDMA_MTagID[2:0]</i>	I	Transaction tag identifier.																				
<i>OC_IDMA_MAddr[31:3]</i>	I	Physical doubleword address bus. This address should fall in the address range programmed in the ISPRAM module.																				
<i>OC_IDMA_MDataValid</i>	I	Write data ( <i>OC_DMA_MData</i> ) valid indication																				
<i>OC_IDMA_MDataTagID[2:0]</i>	I	Write data tag identifier																				
<i>OC_IDMA_MData[63:0]</i>	I	Write data bus to the instruction scratchpad RAM																				
<i>OC_IDMA_SResp[1:0]</i>	O	Read/Write response (00=NULL, 01=VALID 11=ERR)																				
<i>OC_IDMA_STagID[2:0]</i>	O	Return transaction tag ID.																				
<i>OC_IDMA_SData[63:0]</i>	O	Return data read from the scratchpad RAM.																				



Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description
<i>OC_IDMA_SCmdAccept</i>	O	Flow control for commands (0=BUSY, 1=READY) <ul style="list-style-type: none"> <li>The core deasserts this signal when it is not ready to accept a new command. The master has to hold the new command till it is accepted by the core.</li> <li>The core asserts this signal when it has accepted a new command</li> </ul>
<i>OC_IDMA_SDataAccept</i>	O	Flow control for data (0=BUSY, 1=READY) <ul style="list-style-type: none"> <li>The core deasserts this signal when it is not ready to accept a the data driven in <i>OC_IDMA_SData</i>. The master has to hold the data till it is accepted by the core.</li> <li>The core asserts this signal when it has accepted the data driven in <i>OC_IDMA_SData</i></li> </ul>
<b>EJTAG Interface</b>		
TAP interface. These signals comprise the EJTAG Test Access Port.		
<i>EJ_TRST_N</i>	I	Active-low Test Reset Input (TRST*) for the EJTAG TAP. At power-up, the assertion of <i>EJ_TRST_N</i> causes the TAP controller to be reset.
<i>EJ_TCK</i>	I	Test Clock Input (TCK) for the EJTAG TAP.
<i>EJ_TMS</i>	I	Test Mode Select Input (TMS) for the EJTAG TAP.
<i>EJ_TDI</i>	I	Test Data Input (TDI) for the EJTAG TAP.
<i>EJ_TDO</i>	O	Test Data Output (TDO) for the EJTAG TAP.
<i>EJ_TDOzstate</i>	O	Drive indication for the output of TDO for the EJTAG TAP at chip level: 1: The TDO output at chip level must be in Z-state 0: The TDO output at chip level must be driven to the value of <i>EJ_TDO</i> IEEE Standard 1149.1-1990 defines TDO as a 3-stated signal. To avoid having a 3-state core output, the 24Kc core outputs this signal to drive an external 3-state buffer.
<i>Debug Interrupt:</i>		
<i>EJ_DINTsup</i>	S	Value of DINTsup for the Implementation register. When high, this signal indicates that the EJTAG probe can use the DINT signal to interrupt the processor.
<i>EJ_DINT</i>	A	Debug exception request when this signal is asserted one clock period after being deasserted in the previous clock period. The request is cleared when debug mode is entered. Requests when in debug mode are ignored.
<i>Debug Mode Indication:</i>		
<i>EJ_DebugM</i>	O	Asserted when the core is in Debug Mode. This can be used to bring the core out of a low power mode. In systems with multiple processor cores, this signal can be used to synchronize the cores when debugging.
<i>Device ID bits:</i>		
These inputs provide an identifying number visible to the EJTAG probe. These inputs are always available for soft core customers. On hard cores, the core “hardener” can set these inputs to their own values.		

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description																		
<i>EJ_ManufID[10:0]</i>	S	Value of the ManufID[10:0] field in the Device ID register. As per IEEE 1149.1-1990 section 11.2, the manufacturer identity code shall be a compressed form of JEDEC standard manufacturer's identification code in the JEDEC Publications 106, which can be found at: <a href="http://www.jedec.org/">http://www.jedec.org/</a> ManufID[6:0] bits are derived from the last byte of the JEDEC code by discarding the parity bit. ManufID[10:7] bits provide a binary count of the number of bytes in the JEDEC code that contain the continuation character (0x7F). Where the number of continuations characters exceeds 15, these 4 bits contain the modulo-16 count of the number of continuation characters.																		
<i>EJ_PartNumber[15:0]</i>	S	Value of the PartNumber[15:0] field in the Device ID register.																		
<i>EJ_Version[3:0]</i>	S	Value of the Version[3:0] field in the Device ID register.																		
<i>System Implementation Dependent Outputs:</i>																				
These signals come from EJTAG control registers. They have no effect on the core, but can be used to give EJTAG debugging software additional control over the system.																				
<i>EJ_SRstE</i>	O	Soft Reset Enable. EJTAG can deassert this signal if it wants to mask soft resets. If this signal is deasserted, none, some, or all soft reset sources are masked.																		
<i>EJ_PerRst</i>	O	Peripheral Reset. EJTAG can assert this signal to request the reset of some or all of the peripheral devices in the system.																		
<i>EJ_PrRst</i>	O	Processor Reset. EJTAG can assert this signal to request that the core be reset. This can be fed into the <i>SI_Reset</i> signal.																		
<i>TCtrace Interface</i>																				
These signals enable an interface to optional off-chip trace memory. The TCtrace interface connects to the Probe Interface Block (PIB) which in turn connects to the physical off-chip trace pins. Note that if on-chip trace memory is used, access occurs via the EJTAG TAP interface, and use of this interface is not required.																				
<i>TC_ClockRatio[2:0]</i>	O	Clock ratio. This is the clock ratio set by software in <i>TCBCONTROLB.CR</i> . The value will be within the boundaries defined by <i>TC_CRMax</i> and <i>TC_CRMin</i> . The table below shows the encoded values for clock ratio. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>TC_ClockRatio</th> <th>Clock Ratio</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8:1 (Trace clock is eight times the core clock)</td> </tr> <tr> <td>001</td> <td>4:1 (Trace clock is four times the core clock)</td> </tr> <tr> <td>010</td> <td>2:1 (Trace clock is double the core clock)</td> </tr> <tr> <td>011</td> <td>1:1 (Trace clock is same as the core clock)</td> </tr> <tr> <td>100</td> <td>1:2 (Trace clock is one half the core clock)</td> </tr> <tr> <td>101</td> <td>1:4 (Trace clock is one fourth the core clock)</td> </tr> <tr> <td>110</td> <td>1:6 (Trace clock is one sixth the core clock)</td> </tr> <tr> <td>111</td> <td>1:8 (Trace clock is one eight the core clock)</td> </tr> </tbody> </table>	TC_ClockRatio	Clock Ratio	000	8:1 (Trace clock is eight times the core clock)	001	4:1 (Trace clock is four times the core clock)	010	2:1 (Trace clock is double the core clock)	011	1:1 (Trace clock is same as the core clock)	100	1:2 (Trace clock is one half the core clock)	101	1:4 (Trace clock is one fourth the core clock)	110	1:6 (Trace clock is one sixth the core clock)	111	1:8 (Trace clock is one eight the core clock)
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110	1:6 (Trace clock is one sixth the core clock)																			
111	1:8 (Trace clock is one eight the core clock)																			
<i>TC_CRMax[2:0]</i>	S	Maximum clock ratio supported. This static input sets the CRMax field of the <i>TCBCONFIG</i> register. It defines the capabilities of the Probe Interface Block (PIB) module. This field determines the minimum value of <i>TC_ClockRatio</i> .																		

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description														
<i>TC_CRMin[2:0]</i>	S	Minimum clock ratio supported. This input sets the CRMin field of the <i>TCBCONFIG</i> register. It defines the capabilities of the PIB module. This field determines the maximum value of <i>TC_ClockRatio</i> .														
<i>TC_ProbeWidth[1:0]</i>	S	<p>This static input will set the PW field of the <i>TCBCONFIG</i> register.</p> <p>If this interface is not driving a PIB module, but some chip-level TCB-like module, then this field should be set to 2'b11 (reserved value for PW).</p> <table border="1"> <thead> <tr> <th>TC_ProbeWidth</th> <th>Number physical data pin on PIB</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>4 bits</td> </tr> <tr> <td>01</td> <td>8 bits</td> </tr> <tr> <td>10</td> <td>16 bits</td> </tr> <tr> <td>11</td> <td>Not directly to PIB</td> </tr> </tbody> </table>	TC_ProbeWidth	Number physical data pin on PIB	00	4 bits	01	8 bits	10	16 bits	11	Not directly to PIB				
TC_ProbeWidth	Number physical data pin on PIB															
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01	8 bits															
10	16 bits															
11	Not directly to PIB															
<i>TC_PibPresent</i>	S	Must be asserted when a PIB is attached to the TC Interface. When de-asserted (low) all the other inputs are disregarded.														
<i>TC_TrEnable</i>	O	Trace Enable, when asserted the PIB must start running its output clock and can expect valid data on all other outputs.														
<i>TC_Calibrate</i>	O	<p>This signal is asserted when the Cal bit in the <i>TCBCONTROLB</i> register is set.</p> <p>For a simple PIB which only serves one TCB, this pin can be ignored. For a multi-core capable PIB which also uses <i>TC_Valid</i> and <i>TC_Stall</i>, the PIB must start producing the calibration pattern when this signal is asserted.</p>														
<i>TC_DataBits[2:0]</i>	I	<p>This input identifies the number of bits picked up by the probe interface module in each “cycle”.</p> <p>If <i>TC_ClockRatio</i> indicates a clock-ratio higher than 1:2, then clock multiplication in the Probe logic is used. The “cycle” is equal to each core clock cycle.</p> <p>If <i>TC_ClockRatio</i> indicates a clock-ratio lower than or equal to 1:2, then “cycle” is (clock-ratio * 2) of the core clock cycle. For example, with a clock ratio of 1:2, a “cycle” is equal to core clock cycle; with a clock ratio of 1:4, a “cycle” is equal to one half of core clock cycle.</p> <p>This input controls the down-shifting amount and frequency of the trace word on <i>TC_Data[63:0]</i>. The bit width and the corresponding <i>TC_DataBits</i> value is shown in the table below.</p> <table border="1"> <thead> <tr> <th><i>TC_DataBits[2:0]</i></th> <th>Probe uses following bits from <i>TC_Data</i> each cycle</th> </tr> </thead> <tbody> <tr> <td>000</td> <td><i>TC_Data[3:0]</i></td> </tr> <tr> <td>001</td> <td><i>TC_Data[7:0]</i></td> </tr> <tr> <td>010</td> <td><i>TC_Data[15:0]</i></td> </tr> <tr> <td>011</td> <td><i>TC_Data[31:0]</i></td> </tr> <tr> <td>100</td> <td><i>TC_Data[63:0]</i></td> </tr> <tr> <td>Others</td> <td>Unused</td> </tr> </tbody> </table> <p>This input might change as the value on <i>TC_ClockRatio[2:0]</i> changes.</p>	<i>TC_DataBits[2:0]</i>	Probe uses following bits from <i>TC_Data</i> each cycle	000	<i>TC_Data[3:0]</i>	001	<i>TC_Data[7:0]</i>	010	<i>TC_Data[15:0]</i>	011	<i>TC_Data[31:0]</i>	100	<i>TC_Data[63:0]</i>	Others	Unused
<i>TC_DataBits[2:0]</i>	Probe uses following bits from <i>TC_Data</i> each cycle															
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Others	Unused															

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description						
<i>TC_Valid</i>	O	Asserted when a valid new trace word is started on the <i>TC_Data[63:0]</i> signals. <i>TC_Valid</i> is only asserted when <i>TC_DataBits</i> is 100.						
<i>TC_Stall</i>	I	When asserted, a new <i>TC_Valid</i> in the following cycle is stalled. <i>TC_Valid</i> is still asserted, but the <i>TC_Data</i> value and <i>TC_Valid</i> are held static, until the cycle after <i>TC_Stall</i> is sampled low. <i>TC_Stall</i> is only sampled in the cycle before a new <i>TC_Valid</i> cycle, and only when <i>TC_DataBits</i> is 100, indicating a full word of <i>TC_Data</i> .						
<i>TC_Data[63:0]</i>	O	Trace word data. The value on this 64-bit interface is shifted down as indicated in <i>TC_DataBits[2:0]</i> . In the first cycle where a new trace word is valid on all the bits and <i>TC_DataBits[2:0]</i> is 100, <i>TC_Valid</i> is also asserted. The Probe Interface Block (PIB) will only be connected to [(N-1):0] bits of this output bus. N is the number of bits picked up by the PIB in each core clock cycle. For clock ratios 1:2 and lower, N is equal to the number of physical trace pins (legal values of N are 4, 8, or 16). For higher clock ratios, N is larger than the number of physical trace pins.						
<i>TC_ProbeTrigIn</i>	A	Rising edge trigger input. The source should be the Probe Trigger input. The input is considered asynchronous; i.e., it is double registered in the core.						
<i>TC_ProbeTrigOut</i>	O	Single cycle (relative to the “cycle” defined the description of <i>TC_DataBits</i> ) high strobe, trigger output. The target of this trigger is intended to be the external probe’s trigger output.						
<i>TC_ChipTrigIn</i>	A	Rising edge trigger input. The source should be on-chip. The input is considered asynchronous; i.e., it is double registered in the core.						
<i>TC_ChipTrigOut</i>	O	Single cycle (relative to core clock) high strobe, trigger output. The target of this trigger is intended to be an on-chip unit.						
<b>Memory BIST Interface</b>								
These signals provide the interface to optional integrated or user-specified memory BIST capability for testing the SRAM arrays within the core.								
<i>MB_invoke</i>	I	Enable signal for integrated BIST controllers.						
<i>MB_ic_algorithm[7:0]</i>	S	Algorithm selection for I-Cache BIST controllers. For a core configured with IFA-13 BIST support for the I-Cache, bit0 is used to select the BIST algorithm: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th><i>MB_ic_algorithm[0]</i></th> <th>I-Cache BIST Algorithm</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>March-C+</td> </tr> <tr> <td>1</td> <td>IFA-13</td> </tr> </tbody> </table> <p>If the IFA-13 algorithm is selected, then <i>MB_ic_algorithm[5:1]</i> is used to determine the retention delay.</p>	<i>MB_ic_algorithm[0]</i>	I-Cache BIST Algorithm	0	March-C+	1	IFA-13
<i>MB_ic_algorithm[0]</i>	I-Cache BIST Algorithm							
0	March-C+							
1	IFA-13							
<i>MB_dc_algorithm[7:0]</i>	S	Algorithm selection for D-Cache BIST controllers. For a core configured with IFA-13 BIST support for the D-Cache, bit0 is used to select the BIST algorithm: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th><i>MB_dc_algorithm[0]</i></th> <th>D-Cache BIST Algorithm</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>March-C+</td> </tr> <tr> <td>1</td> <td>IFA-13</td> </tr> </tbody> </table> <p>If the IFA-13 algorithm is selected, then <i>MB_dc_algorithm[5:1]</i> is used to determine the retention delay.</p>	<i>MB_dc_algorithm[0]</i>	D-Cache BIST Algorithm	0	March-C+	1	IFA-13
<i>MB_dc_algorithm[0]</i>	D-Cache BIST Algorithm							
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Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description						
<i>MB_sp_algorithm[7:0]</i>	S	<p>Algorithm selection for data scratchpad (DSPRAM) BIST controllers. For a core configured with IFA-13 BIST support for the data scratchpad RAM, bit0 is used to select the BIST algorithm:</p> <table border="1"> <thead> <tr> <th><i>MB_sp_algorithm[0]</i></th> <th>DSPRAM BIST Algorithm</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>March-C+</td> </tr> <tr> <td>1</td> <td>IFA-13</td> </tr> </tbody> </table> <p>If the IFA-13 algorithm is selected, then <i>MB_sp_algorithm[5:1]</i> is used to determine the retention delay.</p>	<i>MB_sp_algorithm[0]</i>	DSPRAM BIST Algorithm	0	March-C+	1	IFA-13
<i>MB_sp_algorithm[0]</i>	DSPRAM BIST Algorithm							
0	March-C+							
1	IFA-13							
<i>MB_isp_algorithm[7:0]</i>	S	<p>Algorithm selection for instruction scratchpad (ISPRAM) BIST controllers. For a core configured with IFA-13 BIST support for the data scratchpad RAM, bit0 is used to select the BIST algorithm:</p> <table border="1"> <thead> <tr> <th><i>MB_isp_algorithm[0]</i></th> <th>DSPRAM BIST Algorithm</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>March-C+</td> </tr> <tr> <td>1</td> <td>IFA-13</td> </tr> </tbody> </table> <p>If the IFA-13 algorithm is selected, then <i>MB_isp_algorithm[5:1]</i> is used to determine the retention delay.</p>	<i>MB_isp_algorithm[0]</i>	DSPRAM BIST Algorithm	0	March-C+	1	IFA-13
<i>MB_isp_algorithm[0]</i>	DSPRAM BIST Algorithm							
0	March-C+							
1	IFA-13							
<i>MB_tr_algorithm[7:0]</i>	S	<p>Algorithm selection for trace memory BIST controllers. For a core configured with IFA-13 BIST support for the trace memory, bit0 is used to select the BIST algorithm:</p> <table border="1"> <thead> <tr> <th><i>MB_tr_algorithm[0]</i></th> <th>Trace mem BIST Algorithm</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>March-C+</td> </tr> <tr> <td>1</td> <td>IFA-13</td> </tr> </tbody> </table> <p>If the IFA-13 algorithm is selected, then <i>MB_tr_algorithm[5:1]</i> is used to determine the retention delay.</p>	<i>MB_tr_algorithm[0]</i>	Trace mem BIST Algorithm	0	March-C+	1	IFA-13
<i>MB_tr_algorithm[0]</i>	Trace mem BIST Algorithm							
0	March-C+							
1	IFA-13							
<i>MB_done</i>	O	Common completion indicator for all integrated BIST sequences.						
<i>MB_dd_fail</i>	O	When high, indicates that the BIST test failed on the data cache data array.						
<i>MB_dt_fail</i>	O	When high, indicates that the BIST test failed on the data cache tag array.						
<i>MB_dw_fail</i>	O	When high, indicates that the BIST test failed on the data cache way select array.						
<i>MB_id_fail</i>	O	When high, indicates that the BIST test failed on the instruction cache data array.						
<i>MB_it_fail</i>	O	When high, indicates that the BIST test failed on the instruction cache tag array.						
<i>MB_iw_fail</i>	O	When high, indicates that the BIST test failed on the instruction cache way select array.						
<i>MB_sp_fail</i>	O	When high, indicates that the BIST test failed on the data SPRAM array.						
<i>MB_isp_fail</i>	O	When high, indicates that the BIST test failed on the instruction SPRAM array.						
<i>MB_tr_fail</i>	O	When high, indicates that the BIST test failed on the trace memory array.						
<i>MB_tombt[n-1:0]</i>	I	Variable width input bus available for user-specified BIST applications.						
<i>MB_frommbt[n-1:0]</i>	O	Variable width output bus available for user-specified BIST applications.						
<b>Scan Test Interface</b>								

Table 17 24Kc™ Core Signal Descriptions (Continued)

Signal Name	Type	Description
These signals provide an interface for testing the core. The use and configuration of these pins are implementation-dependent.		
<i>gscanenable</i>	I	This signal should be asserted while scanning vectors into or out of the core. The <i>gscanenable</i> signal must be deasserted during normal operation and during capture clocks in test mode.
<i>gscanmode</i>	I	This signal should be asserted during all scan testing both while scanning and during capture clocks. The <i>gscanmode</i> signal must be deasserted during normal operation.
<i>gscanramwr</i>	I	This signal controls the read and write strobes to the cache SRAM when <i>gscanmode</i> is asserted.
<i>gscanin[n-1:0]</i>	I	These signal(s) are the inputs to the scan chain(s).
<i>gscanout[n-1:0]</i>	O	These signal(s) are the outputs from the scan chain(s).

## OCP Interface Transactions

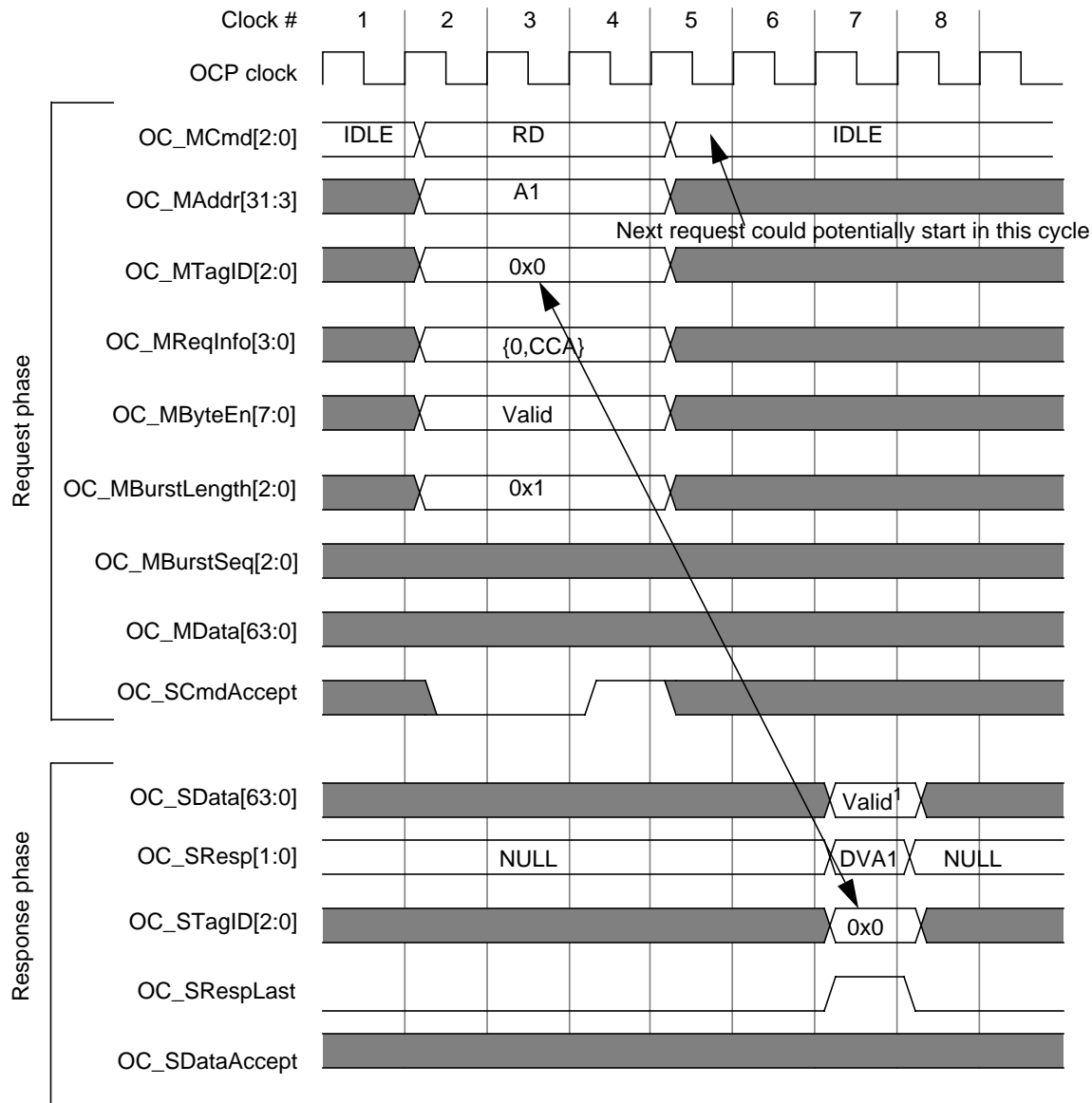
The following sections show timing diagrams for various OCP transactions.

The 24Kc core assumes that any agent or interconnect between it and the target (including the target) can re-order the transactions only if they take on the responsibility of resolving hazards/dependencies.

In a straightforward implementation of an OCP interconnect, the interconnect is expected not to re-order the transactions, but maintain the tagged interface all the way to the target. This essentially gives the transactions a tagging semantic so that Out Of Order (OOO) transaction return is supported. Note that the target is still responsible for checking hazards if it returns responses OOO.

## Single Read

Figure 12 shows a single read transaction, as would occur on an uncached fetch or load. The 24Kc core starts a request phase on clock 2 by switching the MCcmd field from IDLE to RD. Simultaneously, it presents valid values on the address (*OC\_MAddr*), tag (*OC\_MTagID*), transaction info (*OC\_MReqInfo*), byte enables (*OC\_MByteEn*) and burst length (*OC\_MBurstLength*). The slave is shown to flow control the master for one clock then accept the request by asserting *OC\_SCmdAccept* in cycle 4, ending the request phase. The slave responds to this request in cycle 7 with a DVA on *OC\_SResp*, valid data on *OC\_SData*, the return tag ID on *OC\_STagID* and last burst indication on *OC\_SRespLast*. The request phase for a new transaction by the 24Kc core can potentially start in cycle 5.



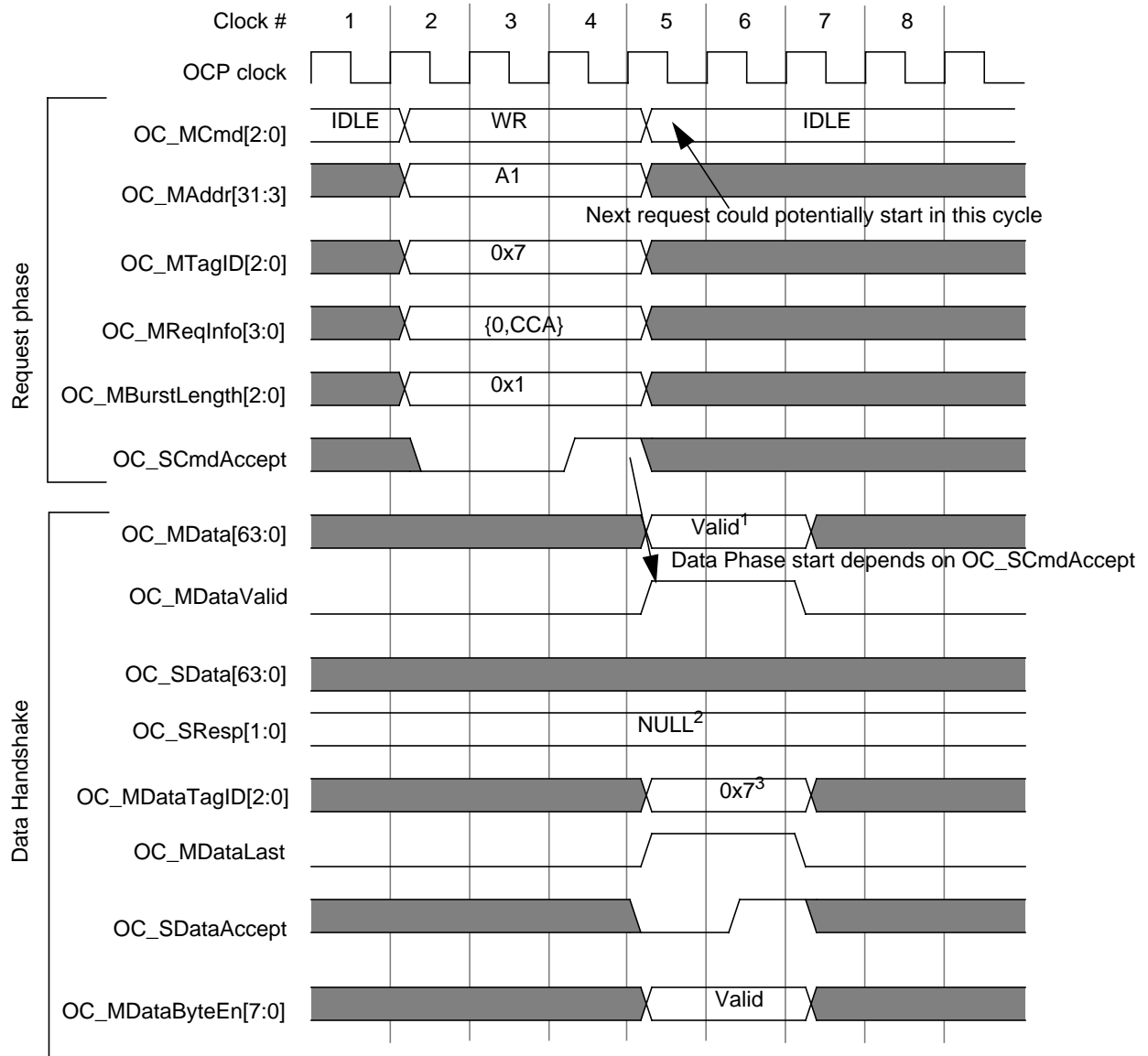
<sup>1</sup> Only the relevant bytes of OC\_SData[63:0] carry valid data corresponding to the request signal OC\_MByteEn[7:0] at the time of request.

Figure 12 Single OCP Read Transaction with flow control

### Single Write

Figure 13 shows a single write transaction which could be generated from an uncached store, or a write-through or uncached accelerated store that does not merge. The 24Kc core starts a request phase on clock 2 by switching the MCmd field from IDLE to WR. At the same time it presents valid values on the address (OC\_MAddr), tag

(OC\_MTagID), transaction info (OC\_MReqInfo), and burst length (OC\_MBurstLength). The data part of the transaction starts when the 24Kc core asserts the OC\_MDataValid in cycle 5 along with the data on OC\_MData and byte enables on OC\_MDataByteEn. The slave is shown to flow control the data phase (as is the request phase) by deasserting OC\_SDataAccept for one cycle before accepting the transaction in cycle 6. A fixed value of 0x7 is used as a TagID for all writes.



<sup>1</sup> Only the relevant bytes of OC\_MData[63:0] carry valid data corresponding to the request signal OC\_MDataByteEn[7:0] at the time of request.

<sup>2</sup> 24Kc core does not expect a response to a posted write. (Some OCP systems generate a response to posted writes in the same cycle as SCmdAccept).

<sup>3</sup> The core always forces the OC\_MDataTagID[2:0] signal to be 0x7 for writes.

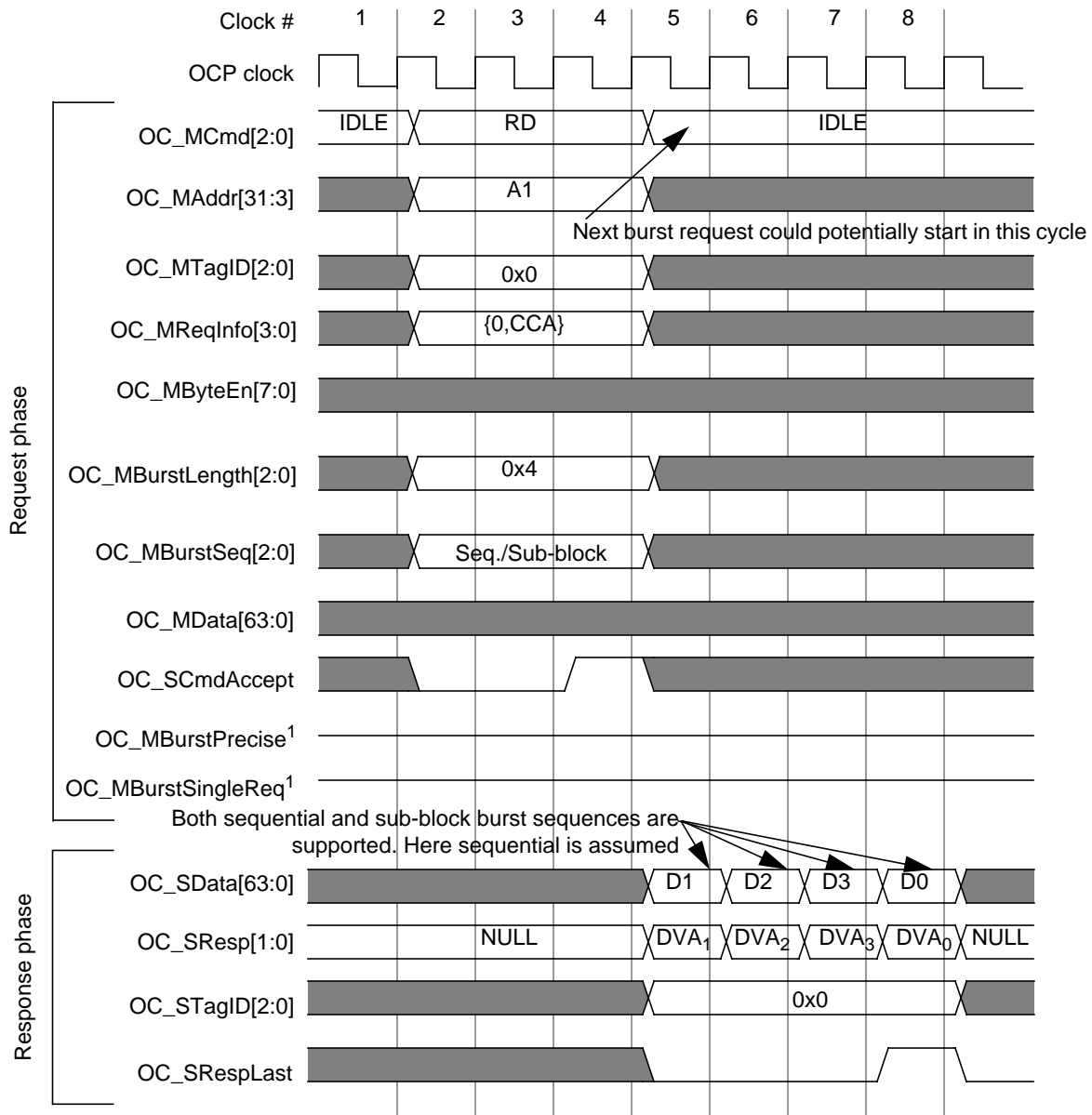
Figure 13 Single OCP Write Transaction with flow control

## Bursted Read

In Figure 14, a bursted read is shown. This is done on a cacheable load or fetch miss to refill the cache line. The

core may be configured for either sequential or sub-block burst order. The transaction looks similar to the single read case except that a burst of four 64b data chunks are transferred in the burst order specified.





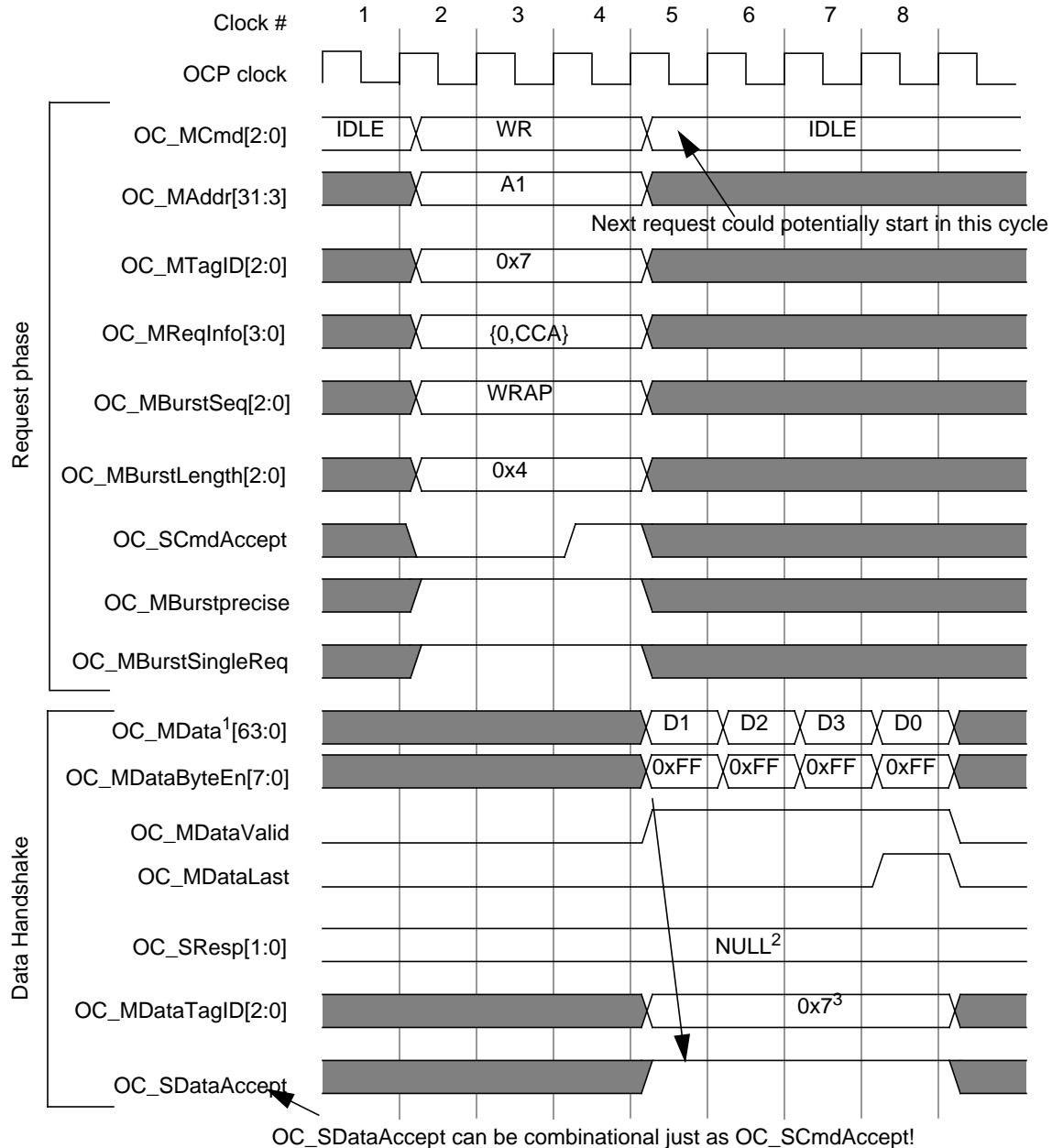
<sup>1</sup> OC\_MBurstPrecise and OC\_MBurstSingleReq are always forced to 0x1 by the 24Kc core since all bursts are precise and only have a single request cycle even if a burst of data is requested.

Figure 14 Burst OCP Read Transaction with flow control

## Bursted Write

Figure 15 depicts a bursted write transaction. This would typically be seen on a dirty cache line write-back, or when uncached accelerated or write-through stores gather an entire line. Bursted writes always begin at the lowest

address of the line. The transaction looks similar to the single write case except that a burst of four 64b data chunks are transferred. Note that the flow control signal *OC\_SDataAccept* can be asserted combinational in cycle 5 as shown.



<sup>1</sup> The 24Kc core will only generate an aligned WRAP burst for burst writes, starting at burst address 0x0.

<sup>2</sup> Core does not expect a response to a posted burst write. (Some OCP systems generate a response to posted writes at the end of the burst, for example an ERR).

<sup>3</sup> Core always forces the OC\_MDataTagID[2:0] signal to be 0x7 for writes.

Figure 15 Burst OCP Write Transaction with flow control

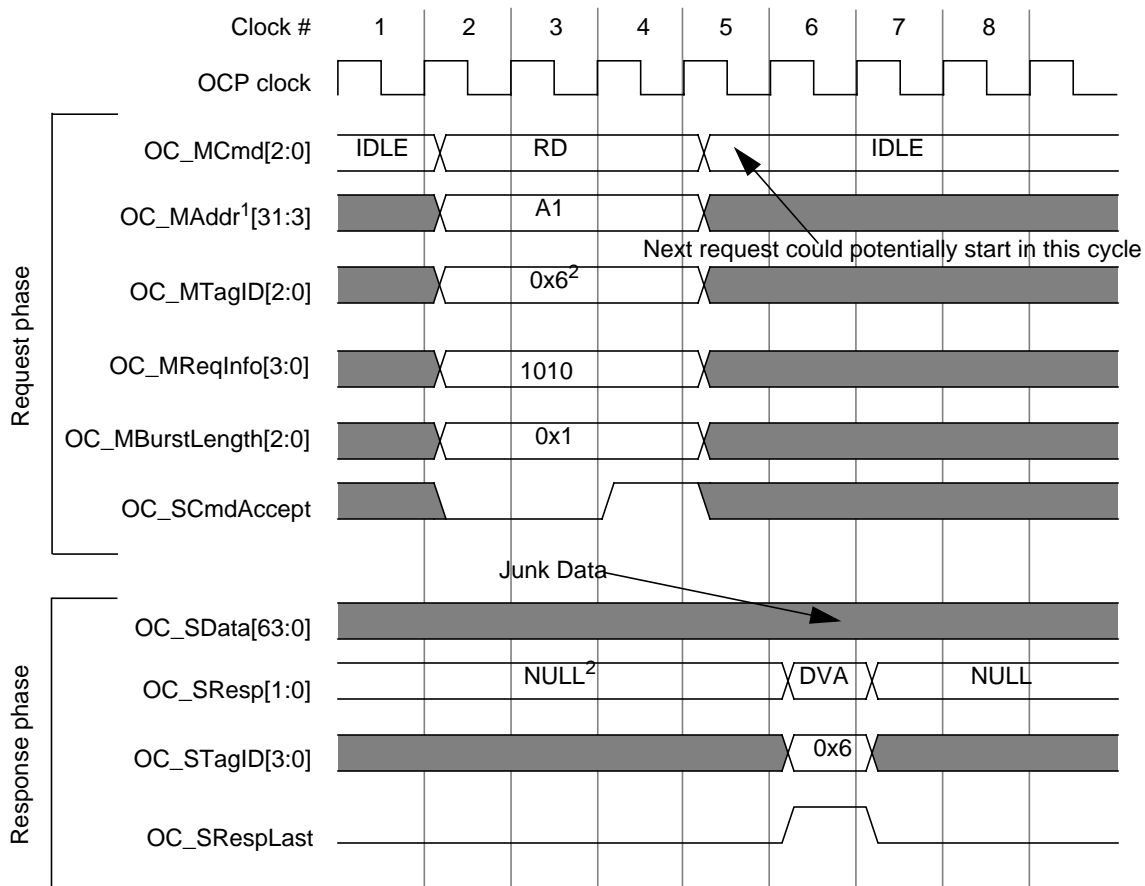
## SYNC Transaction

Figure 16 shows a SYNC transaction. The 24Kc core will only generate this type of transaction for SYNC instructions. The transaction looks very similar to a single read (RD) transaction, along with the following properties:

1.  $OC\_MByteEn$  is 0x0
2.  $OC\_MTagID$  is 0x6

3.  $OC\_MAddr[31:8]$  is 0x1fc000
4.  $OC\_MAddr[7:3]$  carries the SYNC stype bits [10:6]
5.  $OC\_MReqInfo$  is 0xA

The response is shown in clock 6 when the  $OC\_SResp$  bus is asserted by the slave, indicating a DVA (DVA is a valid acknowledgment in OCP terminology).



<sup>1</sup> Since 24Kc cores uses RD for SYNC's, a conservative address (close to the MIPS boot vector) is sent out on  $OC\_MAddr$ . This is a concatenation of {0x1fc000, sync\_opcode\_stype[4:0]}.

<sup>2</sup> Core always forces the  $OC\_MDataTagID[2:0]$  signal to be 0x6 for SYNC's.

Figure 16 SYNC operation as a OCP RD Transaction

## Revision History

In the left hand page margins of this document you may find vertical change bars to note the location of significant changes to this document since its last release. Significant changes are defined as those which you should take note of as you use the MIPS IP. Changes to correct grammar, spelling errors or similar may or may not be noted with change bars. Change bars will be removed for changes which are more than one revision old.

Please note: Limitations on the authoring tools make it difficult to place change bars on changes to figures. Change bars on figure titles are used to denote a potential change in the figure itself. Certain parts of this document (Instruction set descriptions, EJTAG register definitions) are references to Architecture specifications, and the change bars within these sections indicate alterations since the previous version of the relevant Architecture document.

Table 18 Revision History

Revision	Date	Description
00.90	July 17, 2003	Initial version
00.91	July 31, 2003	Updates based on early feedback
00.92	August 8, 2003	Preliminary external release
00.93	September 12, 2003	<ul style="list-style-type: none"> <li>Described several updates to the OCP interface (Thread model, SYNC behavior, MReqInfo, MAddrSpace)</li> <li>Added burst order section</li> <li>Added core-to-bus clocking relationship waveform and description</li> </ul>
00.94	September 29, 2003	<ul style="list-style-type: none"> <li>Removed I/O SError. Use interrupts instead for async bus errors</li> <li>EJ_DINT type should be A</li> <li>Added 4 L2 performance counter signals to I/O list</li> <li>Added sync pattern table to SI_OCPSync in external interface section.</li> </ul>
00.95	December 3, 2003	<ul style="list-style-type: none"> <li>Added Uncached Accelerated flush condition on store to a different 32B region</li> <li>Trademark updates</li> </ul>
01.00	December 10, 2003	<ul style="list-style-type: none"> <li>Updated template</li> </ul>
01.01	January 27, 2004	<ul style="list-style-type: none"> <li>Noted option of running FPU at same clock rate as integer core.</li> <li>Changed names of BIST-related interface signals; they now begin with <i>MB_</i>.</li> <li>Clarified that an OCP write data phase starts one cycle after the command phase is accepted.</li> </ul>
01.02	February 11, 2004	<ul style="list-style-type: none"> <li>Clarified number of possible hardware breakpoints.</li> <li>Fixed document template</li> </ul>
02.00	March 5, 2004	<ul style="list-style-type: none"> <li>Removed unused <i>SI_OCPClkIn</i> input pin.</li> <li>Renamed <i>gscan{in,out}_x</i> pins to <i>gscan{in,out}[n-1:0]</i>.</li> <li>Increased number of parity bits in I-cache data array, if parity is enabled.</li> <li>Updated MDU latencies</li> </ul>
02.01	May 26, 2004	<ul style="list-style-type: none"> <li>Added new static inputs to control selection of integrated memory BIST algorithm.</li> <li>Added <a href="#">Table 14</a> summarizing build-time configuration options.</li> </ul>

Table 18 Revision History

Revision	Date	Description
03.00	September 15, 2004	<ul style="list-style-type: none"> <li>• Described SPRAM and COP2 interfaces.</li> <li>• Added breakpoint status output pins.</li> <li>• Updated OCP interface to OCP version 2.1, with use of TagID fields.</li> </ul>
03.01	November 10, 2004	<ul style="list-style-type: none"> <li>• OCP Sync waveform clarified.</li> <li>• Other minor improvements.</li> </ul>
03.02	March 15, 2005	<ul style="list-style-type: none"> <li>• Described the MIPS Trace interface.</li> <li>• Other minor updates</li> </ul>
03.03	April 26, 2005	<ul style="list-style-type: none"> <li>• Described the ISPRAM interface.</li> <li>• Other minor updates</li> </ul>
03.04	June 30, 2005	<ul style="list-style-type: none"> <li>• Various enhancement updates</li> </ul>

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